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HYBRID MICROCIRCUIT FAILURE RATE PREDICTION

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IITRI/Reliability Analysis Center

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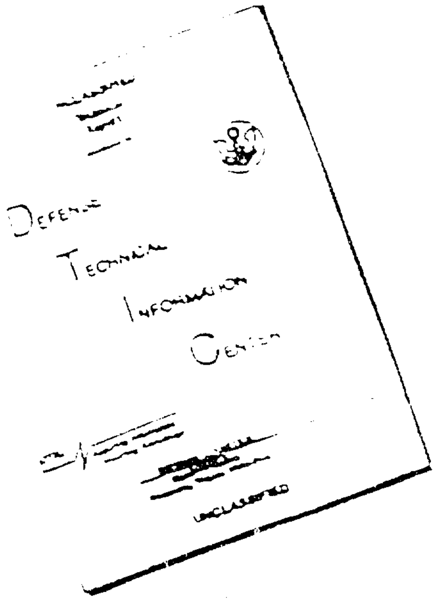

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This report presents an updated reliability prediction model for hybrid microcircuits for inclusion in MIL-HDBK-217B, "Reliability Prediction of Electronic Equipment".

The new model differs in several ways from the previous MIL-HDBK-217B prediction technique. Some of the changes include the addition of a density factor and an interconnection factor; changes in the package factor and quality factor; and individual assessments of the effect of temperature and environment on the elements of the hybrid microcircuits. (Cont'd)

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Comparisons are presented comparing the predicted failure rates to the failure rate experienced by various hybrid microcircuits in the field. Also, the relative contributions of the terms in the model are compared to the distribution of field failure causes.

PREFACE

This final report was prepared by IIT Research Institute, Chicago, IL., as part of Contract F30602-77-C-0167. The work was sponsored by the Rome Air Development Center, Griffiss AFB, New York, with Mr. Peter Manno serving as the RADC Technical Monitor for this program. This report covers work conducted from August 1976 to February 1977.

The principal investigator for this project was Mr. T.E. Turner, with valuable assistance provided by Mr. L.A. Mirth and Mrs. C.A. Proctor. Data used in the analysis were collected by Mr. I.L. Krulac.

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EVALUATION

The objective of this effort was to evaluate and update the hybrid microcircuit failure rate prediction model in MIL-HDBK-217B, "Reliability Prediction of Electronic Equipment."

As a result of this program, a new model was developed which differs in several ways from the previous MIL-HDBK-217B prediction technique. The following are some of the major changes or additions:

a. The effect of temperature and environment cannot be expected to affect all elements within a hyrbid microcircuit equally, thus each element within a hybrid has been given its own temperature and environmental factor rather than one for the hybrid as a whole.

b. A term based on the density of the hybrid was found necessary to account for the effect of the tighter workmanship requirements, finer lines, and the increased processing required for more dense circuits.

c. Interconnection failures were found to have a very significant effect on the overall reliability of the hybrid. The prevalence of these failures necessitated a more sensitive term to account for their effect on the hybrid's failure rate. Bond metallurgy and temperature were found to affect interconnection failure rates.

d. The models for discrete semiconductors, capacitors and integrated circuits presently in MIL-HDBK-217B are utilized within the new model. These models have been adapted for application to dice or chips inside a hybrid package by multiplying by a term to remove the effect of package and interconnection failures from the discrete models.

e. The vast combinations of materials and designs for hybrid packages made generalizations for broad classifications of package types virtually impossible. Package seal perimeter, however, was found to be a significant parameter for all types of packages. The new package term is a function of only the seal perimeter, temperature, and environment.

f. The substrate metallization technology (thin or thick film) was not found to be significant in this study; therefore, the new model does not differentiate between the two technologies.

g. The new model, in accordance with MIL-STD-883B, Method 5008, "Test Methods for Hybrid Microcircuits," establishes only two quality levels for hybrid microcircuits (level B or commercial). However, provision for a Class S quality level has been included and a factor will be assigned when the procurement and screening requirements are established.

Comparisons are presented between the predicted failure rates and the failure rates experienced by various hybrid microcircuits in the field. In addition, sample calculations are included which shows a good correlation when comparing the predictions for an equivalent circuit constructed with discrete devices.

The new model has been coordinated with DOD and industry and has been included in Notice 2 to MIL-HDBK-217B.

Peter F. Manno

PETER F. MANNO
Project Engineer

Section I

INTRODUCTION

1.1 Purpose

The purpose of this effort was to evaluate the hybrid microcircuit failure rate prediction model found in MIL-HDBK-217B, identify those factors most closely correlated with the reliability of a hybrid microcircuit, and if necessary, develop a new model to give a better estimate of the inherent reliability of a hybrid microcircuit.

1.2 Background

The steady increase in the use of hybrid microcircuits in military and commercial systems as well as the increased size of some hybrids has necessitated a simple and accurate method of evaluating the inherent reliability of these devices. Since the publication of MIL-HDBK-217B, 20 September 1974, a substantial body of evidence has surfaced which suggests that the hybrid failure rate prediction model found therein may need to be updated. Areas of contention are:

a. Predictions for particular functions when implemented in hybrid as compared to discrete technologies.

b. Difficulty in making calculations due to complexity.

c. Weighting given to constituent factors.

d. Factors not considered by the model.

Additional changes are necessary in order to be consistent with recently released Method 5008 of MIL-STD-883 and Appendix G to MIL-M-38510 which established only one military quality level rather than the three in MIL-HDBK-217B. The new screening requirements imposed by Method 5008 may be expected to affect the reliability of a hybrid device and thus the quality factors in the model.

This investigation was initiated to either justify the present hybrid prediction model with actual hard data or develop a new model which would more accurately predict the observed failure rates.

Section II

DATA COLLECTION

The only way to evaluate the accuracy of a prediction technique is to compare the prediction for a part to data provided by the actual use of the part. The Reliability Analysis Center, (RAC), in the course of its normal operation, collects failure rate data from both commercial and military users of microelectronic devices. Thus, at the beginning of this study, the RAC data base already contained a substantial amount of information. However, as hybrid microcircuits cover a range from two transistor chips to multilayered complex circuits involving LSI integrated circuits, vast amounts of data are necessary to make an attempt at evaluating or developing a good reliability prediction model. Therefore, an extensive 6-mouth effort by the staff of the Reliability Analysis Center was initiated to collect whatever reliability information was available.

Along with failure rates, detailed descriptions of the microcircuits were necessary. Descriptive factors sought included: number and type of components, component attach method, package size, type and number of leads, package seal/material, number and type of internal interconnections, type of substrate metallization (thin or thick film), number of metallization levels, application (general system function), application environment, substrate material and surface area.

The initial RAC data collection effort, coupled with the data already in the RAC data base totaled approximately 300 million part hours from 320 circuit designs, representing the products of 36 manufacturers. Approximately 40 million additional part hours of data were contributed in response to a letter circulated by Mr. D.F. Barber, Chief, Reliability Branch, Reliability and Compatability Division, Rome Air Development Center. This letter was also circulated by Aerospace Industries Association of America, Inc. Of these 40 million hours, however, only about 10 million hours were usable due to the lack of detailed construction descriptions for many of the microcircuits. These data were mainly the result of actual field operation, although some data resulted from reliability demonstration tests or operating life tests.

A second effort by the RAC, pursued in conjunction with the first, collected failure analysis information from hybrid microcircuits that had failed either in the field or during system level operating tests. Only primary failures were considered. Overstress failures caused by design errors, the failure of another part, or application error were considered secondary failures. Failure analysis of over 200 primary failures were eventually collected.

A small amount of particularly useful field data was collected which gave the failure rates of the microcircuits and also analyzed every reported failure. Unfortunately, however, most of the failure analysis reports were only samples of actual experienced failures. Most failure rate reports gave only a verification of failure without an indication of the cause.

The RAC data base also contains over 5 billion part hours of field, reliability demonstration, and test data from monolithic integrated circuits and discrete semiconductors. This provided useful background information on the devices used within hybrid microcircuits and could be used to evaluate or develop the terms for these devices within the hybrid model.

Most of the hybrid data involved in this study have been published in a compendium entitled Microcircuit Device Reliability - Hybrid Circuit Data (MDR-5) which is available from the Reliability Analysis Center or the National Technical Information Service.

Section III

EVALUATION OF THE HYBRID OF MIL-HDBK-217B

3.1 Critique of the Model

Comments from users of the hybrid prediction model received by the Rome Air Development Center consisted of four general criticisms.

a. If the model is compared to the models for discrete components, it would appear that a circuit constructed as a hybrid would exhibit a lower failure rate than the same circuit constructed of discrete components in one environment, yet would appear considerably less reliable in another environment (see Appendix E, Example 1). This is due to the fact that the hybrid model involves one environmental factor which multiplies the entire base failure rate. The discrete integrated circuit (IC) model, however, is only partially multiplied by the environmental factor. Yet, the environmental factors are equal for both models, and the hybrid model uses the integrated circuit model as part of its base failure rate.

b. The integrated circuit contribution to the hybrid base failure rate is determined using the discrete integrated circuit model assuming an ambient temperature of 25°C. The entire hybrid base failure rate is multiplied by a temperature factor to reflect the operating temperature of the device. This factor results in a much higher predicted failure rate for an IC used in a hybrid than the same IC discretely packaged. For example, a quad 2 input NAND gate chip within a hybrid microcircuit in an airborne uninhabited environment will contribute a term to the base failure rate of the hybrid which will be a factor of 2.1 greater if operated at a junction temperature of 45°C as compared to 25°C. The same chip in a discrete package, however, will show a predicted failure rate which will be only a factor of 1.015 greater at 45°C than at 25°C.

c. Semiconductor dice used in hybrid microcircuits are not normally screened nor fully tested, therefore, the designations JAN, JANTX, and JANTXV are not applicable. Thus, the note at the bottom of Table 2.1.7-3 of MIL-HDBK-217B is very ambiguous. Interpreted rigorously, this would raise the failure contribution of nearly all chip and wire mounted semiconductors by a factor of 5. This seems unreasonably high. Using this factor a PNP linear transistor within a hybrid would contribute more to the base failure rate than would a 741 OP AMP even though both chips had received the same screening (none), and irrespective of the stress ratios.

d. The multiplier factor of 2.0 applicable to all bipolar and MOS linear, bipolar beam lead, bipolar ECL and other MOS devices in Table 2.1.7-3 seems to be a rather stiff penalty. Again, using the example of a quad 2 input NAND gate operated in an airborne uninhabited environment, if a discrete integrated circuit prediction is calculated, it

could be seen that the MOS device would not have a failure rate equal to twice that of a bipolar equivalent unless operated at a junction temperature of 92°C. This temperature is somewhat higher than is normally experienced by most hybrids.

3.2 Predicted vs Experienced Failure Rates

To test the accuracy of the hybrid prediction model of MIL-HDBK-217B, predictions were calculated for devices from which adequate data had been collected. To provide an accurate comparison, it was decided to compare the predicted reliability to data obtained only from actual field operation. Reliability demonstration and life test results were not considered. Data from microcircuits for which the reported part hours were not significantly greater than the average life of the microcircuit (data items reporting no failures or only one failure) were also rejected.

The remaining data has been summarized in Table I. Point estimates were calculated as reported failures divided by part hours. The lower limit (20% limit) is the 20% level of the Chi-square distribution, and the upper limit (80% limit) is the 80% level of the Chi-square distribution. These are the limits of a 60% confidence interval around the point estimate.

Several reports provided only a replacement rate rather than a failure rate. No effort was made to verify that the parts replaced in the field were indeed failed parts. These reports are indicated by an "R" following the point estimate. Experience has shown that the actual failure rate is generally within the range of 50 to 75% and typically 67% of the field replacement rate for military systems. The number below the point estimate followed by an "A" is the adjusted failure rate (equal to 67% of the replacement rate).

A graph comparing the predicted and experienced data is given in Figure 1. The straight diagonal line represents that set of points for which the experienced failure rate exactly equals the predicted failure rate. If the prediction is a good estimate of the experienced, the points should group around this line. The data presented indicate a rather low correlation between the predicted and observed failure rate.

3.3 Weighting of Constituent Factors

The failure analysis reports collected by the Reliability Analysis Center were grouped into categories according to the principal cause of failure. The pie chart in Figure 2 was drawn from these reports. These results are very similar to those presented in a similar study conducted by Hughes Aircraft under contract to the U.S. Army Electronics Command (Ref. 1).

Since Figure 2 represents the distribution of the failures which can be expected, it would seem intuitive that the relative contribution of the factors of the base failure rate should be similar. The most obvious discrepancy between the failure distribution and the base failure rate of the model is the fact that the interconnections are not considered in the model (except in λ_C, the density factor), however, they comprise over 25% of the experienced failures. The model apparently reasons that, since the base failure rate for the

Table 1. OBSERVED vs PREDICTED FAILURE RATES
(PER MIL-HDBK-217B)

Circuit Function	No. Fail.	Part Hour	20% Limit *	Point Estimate *	80% Limit *	Predicted
Temperature Control Voltage Regulator	2	1.26E6	0.654	1.59	3.40	4.69
Delay Driver	12	1.32E6	6.84	9.09	12.0	6.09
Quad Logic Level Converter	4	3.80E6	0.604	1.05	1.77	6.79
Current Driver	38	3.84E7	0.853	0.990	1.15	0.556
Signal Processor (Class C)	8	3.95E5	14.1	20.3R 13.6A	28.8	74.7
12 Bit SSI Register	6	2.54E5	15.1	23.6R 15.8A	35.7	3.99
Dual Voltage Regulator (AU)	14	7.22E5	15.0	19.4R 12.4A	25.1	24.2
Dual Voltage Regulator (AI)	4	4.35E5	5.20	9.20R 6.23A	15.5	16.1
Fault Detector	6	3.94E5	9.91	15.2R 10.2A	23.0	53.1
MCAN Detector Commutated	2	2.44E6	0.338	0.820R 0.547A	1.75	54.3
Detector Fixed	3	2.44E6	0.639	1.23R 0.824A	2.26	16.8
Lamp Driver	3	2.10E5	7.31	14.3R 9.6A	26.3	8.37
FET Switch	5	1.75E7	0.177	0.286E 0.191A	0.452	2.75
Diode Array (Class C)	2	9.50E5	0.868	2.11	4.50	49.3
Mode Logic	5	6.50E5	4.75	7.69	12.2	0.960
Timing Logic	4	6.50E5	3.53	6.15	10.3	0.970

Table 1. OBSERVED vs PREDICTED FAILURE RATES
(PER MIL-HDBK-217B) (Cont'd)

Circuit Function	No. Fail.	Part Hour	20% Limit*	Point Estimate*	80% Limit*	Predicted
Logic Sequencer	4	6.50E5	3.53	6.15	10.3	0.945
Mode Control	7	6.50E5	7.28	10.8	15.7	0.952
Word Masking Logic	2	6.50E5	1.27	3.08	6.58	0.976
Interface Driver	12	3.50E6	2.58	3.43	4.54	3.26
Interface Driver	3	5.80E5	2.65	5.17	9.51	2.47
Data Buffer	17	2.30E6	5.86	7.39	9.32	2.19
Buffer	2	5.80E5	1.42	3.45	7.38	1.29
Timing Control	6	6.51E5	6.01	9.23	14.0	0.774
Memory Hybrid Switch	31	1.40E8	0.187	0.221	0.262	3.86

R Indicates Removal Rate

A Indicates Failure Rate (67% of Removal Rate)

* Failures/Million Hours

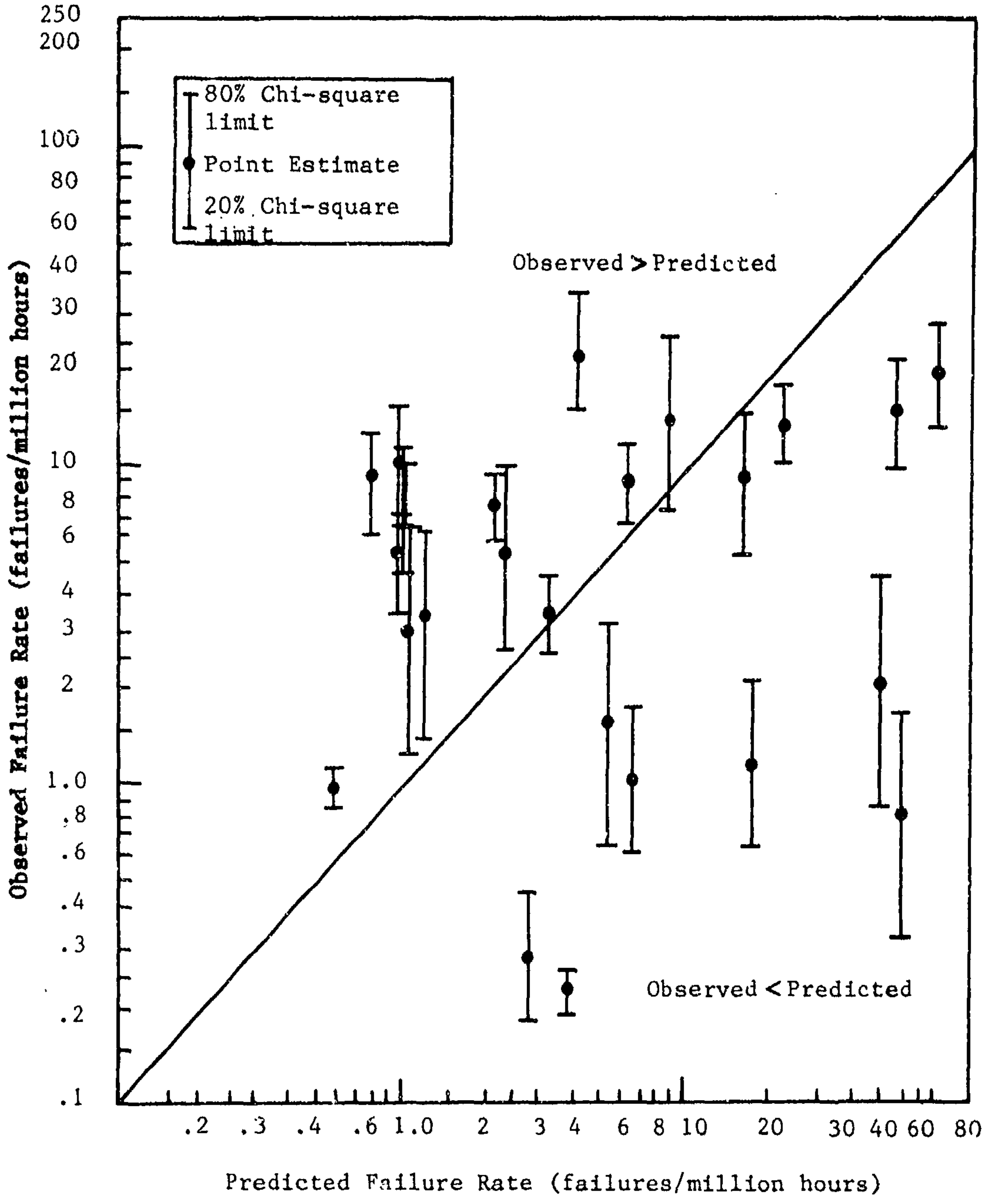


Figure 1: Observed Failure Rate vs Predicted Failure Rate (see Table 1) Calculated per MIL-HDBK-217B (20 Sept. 74)

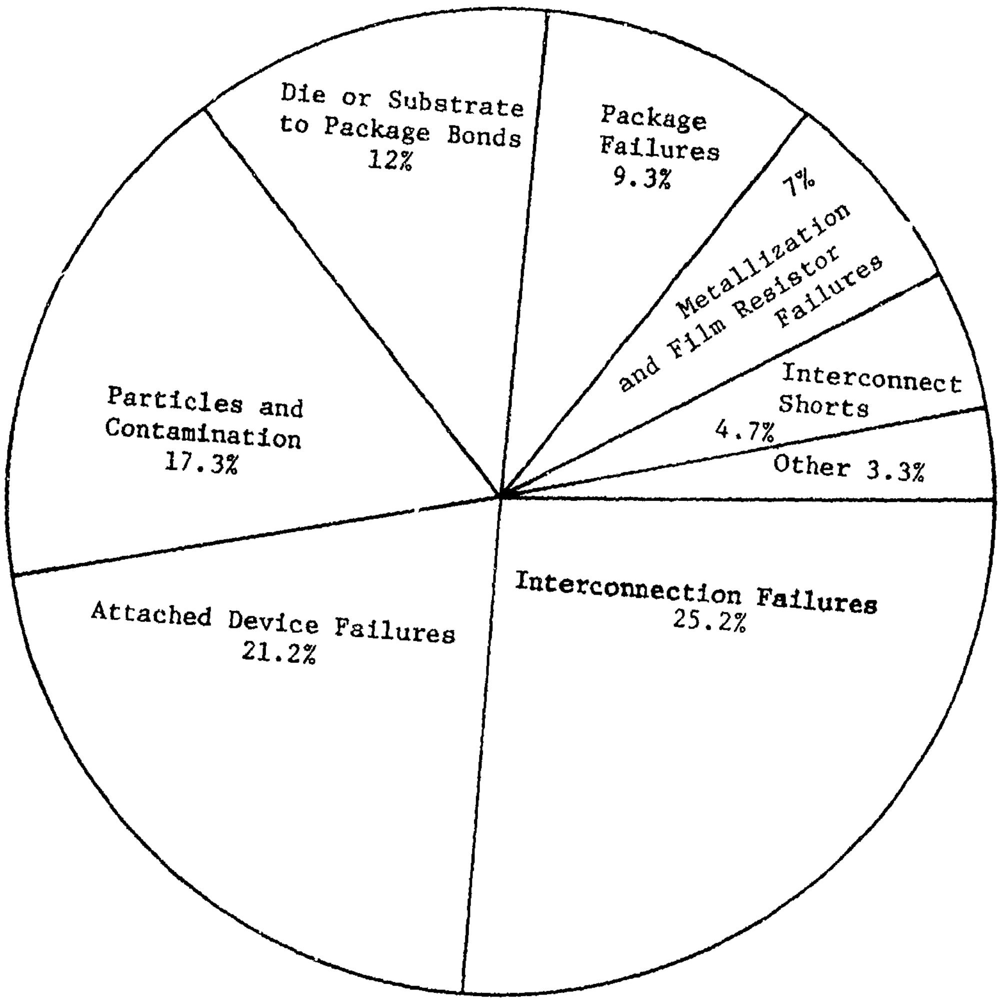


Figure 2: Failure Mode Distribution

hybrid model is based on factors for discretely packaged components, the failure rates for the interconnections to any component should be included in the failure rate contribution of that component. This assumption does not consider the interconnections necessary to connect the hybrid substrate metallization to the lead frame, nor any substrate metallization to substrate metallization jumper wires often used in hybrid microcircuits. It does, however, include the contribution of discrete package failures, even though discrete package failures are irrelevant to the reliability of the hybrid. λ_c considers the actual number of bonds. However, this number is only used as an indication of complexity to arrive at a substrate failure contribution, rather than a bond contribution. If λ_c was interpreted as a bond failure rate, the assigned value for this term would seem to be very optimistic.

Continuing the comparison of the failure distribution to the base failure rate, it soon became obvious that the failure data must be reclassified. Categories created were "passive component" and "substrate to lead frame bonds". Die bond failures were considered to be failures of the components, as were wire bond failures, unless the bond was not to a component, in which case it was classified as "substrate to lead frame bond". Interconnect shorts were considered the same as interconnect failures. Contamination and particle failures were classified as belonging to the category of the component contaminated, and substrate bond failures were considered substrate failures. The new failure mode distribution appears in Figure 3.

The relative weighting of the base failure rate was calculated by summing the individual factors of the base failure rates of all the devices in the data base. The factors are shown in Figure 4. Comparing Figure 3 to Figure 4 reveals that the MIL-HDBK-217B model apparently overweights the active device contribution while underweighting the passive components.

3.4 Evaluation Summary

A comparison of the predicted failure rate to the failure rate that was actually experienced in the field revealed that some revision to the reliability prediction model in MIL-HDBK-217B was necessary. Comments from various sources in the industry pointed out several inconsistencies in the present model with respect to the:

a. environmental factor
b. temperature factor
c. semiconductor failure rate contribution

Comparing the relative distribution of the factors comprising the predicted base failure rate to the actual failure mode distribution showed that the passive components were underweighted by the model and the active components were apparently overweighted. A term for interconnect failure was also shown to be necessary.

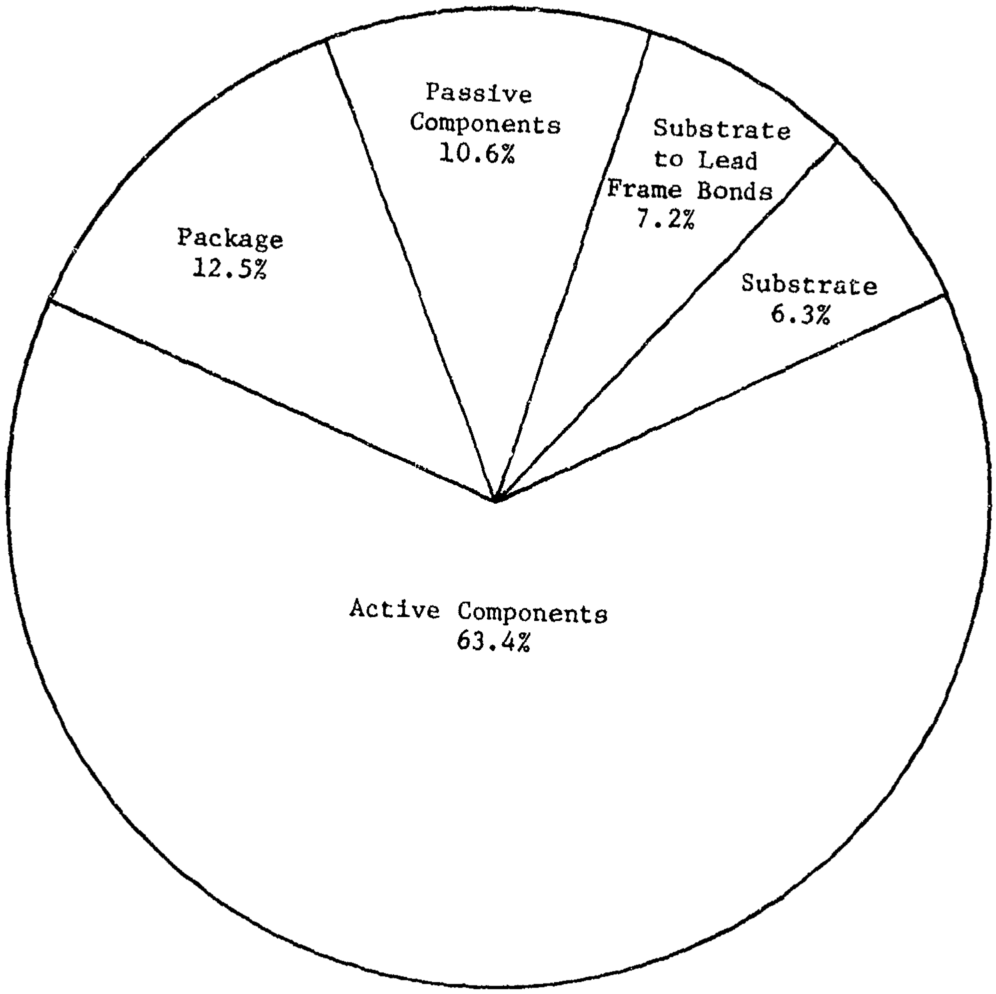


Figure 3: Reclassified Failure Mode Distribution

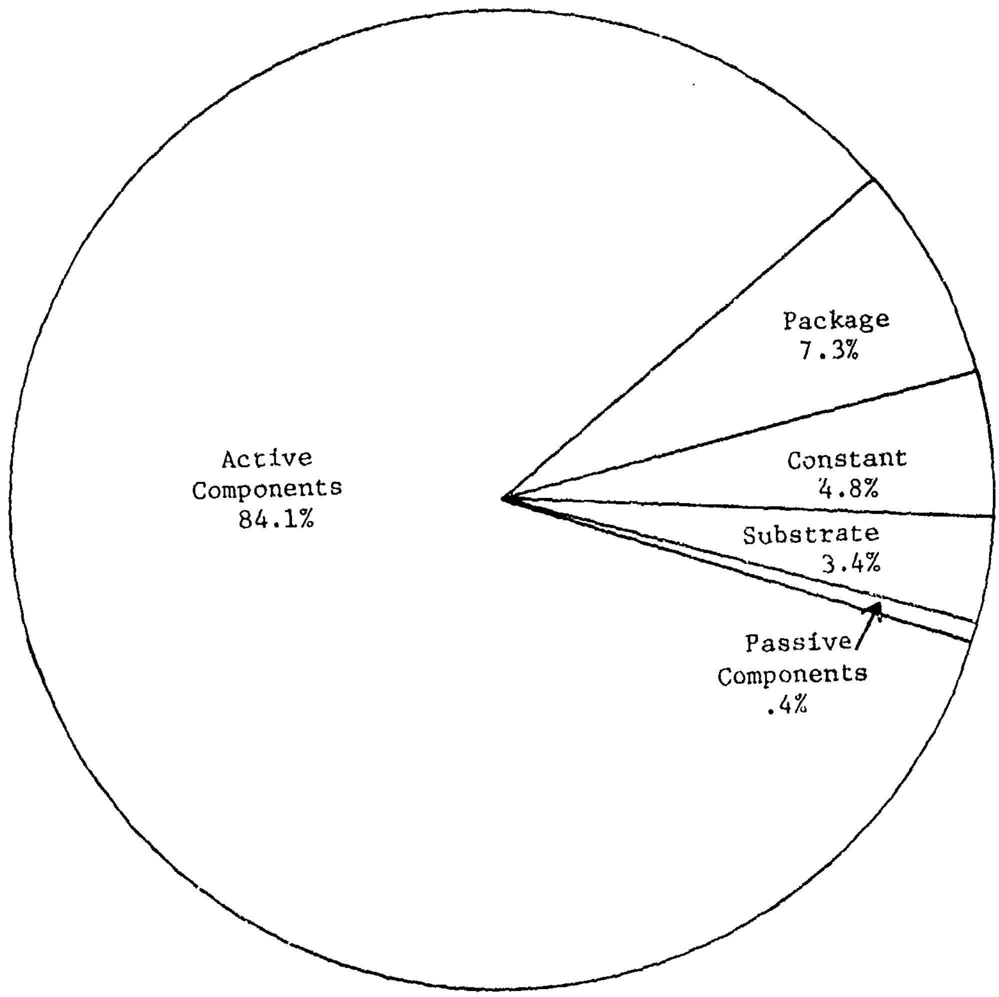


Figure 4: Weighting of Factors in Base Failure Rate
MIL-HDBK-217B

Section IV

DEVELOPMENT OF A NEW MODEL

Having established that a revision to the hybrid microcircuit reliability prediction model found in MIL-HDBK-217B, 20 Sept. 1974 was necessary, and having identified the major sources of disparities in the present model, work was begun to develop a new model.

The initial assumption was made that the failure rate for a hybrid microcircuit will be the sum of the failure rates of its components. Thus, the approach in the model development involved a term by term analysis of the various microcircuit components which might impact the reliability of a component. A preliminary analysis employing multiple linear regression techniques was performed to identify the most significant variables and to evaluate the effects of adopting a constant or more complicated expression to describe each variable. The final analysis utilized actual data to verify each of the model parameters.

4.1 Interconnections

Interconnect failures were the single most frequent cause of failure identified in this study. This fact alone would seem to justify a term for this factor. The model of MIL-HDBK-217B attempted to consider the interconnections along with the attached component failure contributions. This was not completely effective as it did not consider the substrate to lead frame interconnections and it assumed that the effect of temperature was the same for all types of interconnects and dice.

To determine a failure rate contribution of interconnections, field and test data were collected from hybrid and monolithic microcircuits for which all the failures were analyzed. From this a bond failure rate was determined (bond failures/part hours x number of interconnections). The results for bimetal (Au-Al) bonds are given in Table 2 and graphed in Figure 5. The second set of failure rates given for the field data is the failure rate after correcting to a "Ground Benign" environment using the appropriate environmental factors. An Arrhenius curve was fit to these data. Since the data seemed to indicate a dramatic increase above 150°C, two continuous curves were used. The sharp increase above 150°C is probably due to the formation of gold-aluminum intermetallic compounds and its associated voiding above this temperature. The equations fit to these lines are:

$$I_1 = 0.00174 \exp\left[(-5075)\left(\frac{1}{T+273} - \frac{1}{298}\right)\right] \text{ for } T \le 150°C \qquad (4.1.1)$$

$$I_1 = 1.96\times10^{-6} \exp\left[(-9594)\left(\frac{1}{T+273} - \frac{1}{298}\right)\right] \text{ for } T > 150°C \qquad (4.1.2)$$

T = Junction temperature (ΛC)

Interconnections made with single metal bonds (Al-Al, Au-Au, etc.) and solder connections did not exhibit the same temperature dependence. Data from both hybrid and monolithic microcircuits employing single metal or solder interconnections were analyzed to derive bond failure rates. In this case, however, there was not enough data to formulate any credible relationships. In an attempt to obtain more information, the data base was again analyzed to find data for which failure indicators were supplied. These were classified as possible interconnect failures or improbable interconnect failures. Using the existing data, a percentage of possible interconnect failures to actual interconnect failures was calculated. Using this percentage, an interconnect failure rate was estimated for the devices classified as possible interconnect failures. These data are listed in Table 3 and graphed in Figure 6. Again an Arrhenius curve was fit to the data. The equation for the curve is:

$$\lambda_{I_2} = 0.000174 \exp\left[-4056\left(\frac{1}{T + 273} - \frac{1}{298}\right)\right] \qquad (4.1.3)$$

T = Junction temperature (^{o}C)

The data used to arrive at the interconnect failure rate equation were based on the junction temperature of the devices. In the application of the model, however, the individual component junction temperatures may be very difficult to obtain. The external case temperature may be the only thermal measurement readily available. If the case temperature is used to determine the bond failure rate contribution based on the curves in Figures 5 and 6, a large error may be introduced. This error will be due to the rise of junction temperature over the case temperature and thus is a function of the circuit configuration and materials used in the microcircuit. This problem will be discussed further in Section 4.2.

Environmental stresses may also be expected to be important when calculating the reliability of the interconnections. Environmental factors for interconnections are developed in Section 4.6.

4.2 Integrated Circuits

Integrated circuits are used extensively in hybrid microcircuits. The wide variation in complexity and function of common integrated circuits requires that these factors be considered when calculating a failure rate for the ICs. The integrated circuit reliability prediction model, found in Section 2.1 of MIL-HDBK-217B, is the only widely accepted method of calculating such a failure rate. The data in the RAC data base for hermetic SSI and MSI monolithic TTL microcircuits (a mature technology for which there is a good deal of data) indicate a reasonably good correlation between the experienced field failure rate and that predicted per MIL-HDBK-217B. The model, however, is for discretely packaged devices, and thus must consider the failures related to the discrete package and interconnections as well as the die. The failure rate contributions associated with the discrete package and interconnections must be removed from the predicted failure rate in order to determine an accurate die failure rate. Failure analysis reports for monolithic microcircuits were collected and divided into two categories; package and interconnect

Table 2: BI-METALLIC INTERCONNECTION FAILURE RATES

Temp °C	Data Type Environment	Bond Hours	No. Failed	Bond Failure Rate (Fail/10^6 Hr.) 20% Limit	Pt. Estimate	80% Limit
28	Field A_I	1.15E10	8	4.84E-4 1.21E-4	6.95E-4 1.74E-4	9.90E-4 2.48E-4
43	Field A_I	1.81E9	2	4.57E-4 1.14E-4	0.00111 2.78E-4	0.00237 5.93E-4
90	Field G_F	1.73E9	13	0.00573 0.00287	0.00751 0.00376	0.00983 0.00492
125	Test G_B	4.74E8	8	0.0118	0.0168	0.0240
150	Test G_B	9.20E7	2	0.00893	0.0217	0.0465
175	Test G_B	2.69E7	7	0.176	0.260	0.380
200	Test G_B	2.02E7	3	0.0760	0.149	0.273
230	Test G_B	NA	NA	NA	1.25	NA
250	Test G_B	4.42E6	9	1.45	2.04	2.83
275	Test G_B	NA	NA	NA	5.71	NA
325	Test G_B	NA	NA	NA	16.7	NA

NA = Not available, only a failure rate given.

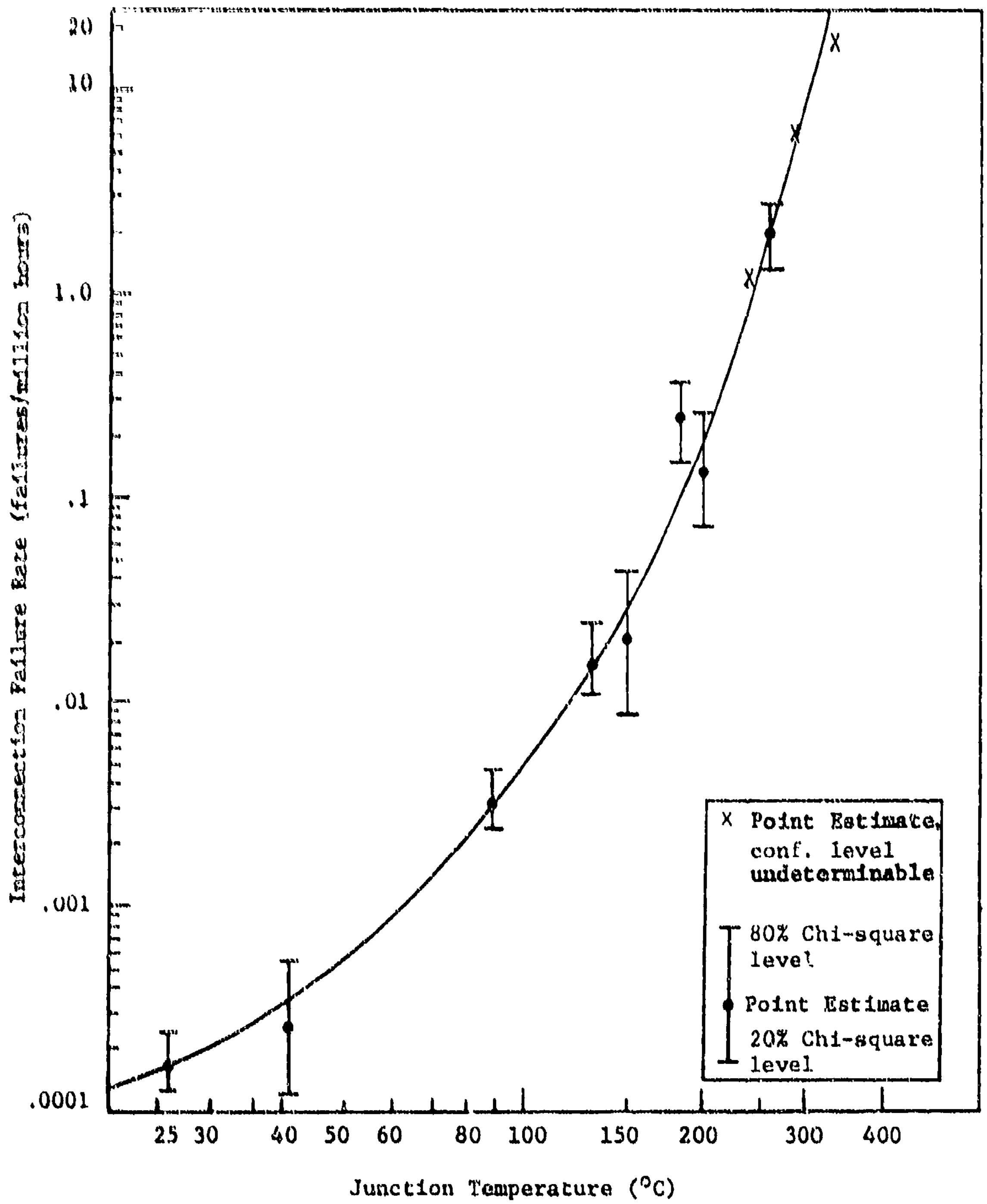


Figure 5: Bi-Metallic Interconnection Failure Rates

Table 3: Single Metal and Solder Interconnection Failure Rates

Temp. °C	Data Type Environment	Bond Hours	No. Failed	Bond Failure Rate (Fail/10^6 Hr.)		
				20% Limit	Pt. Estimate	80% Limit
28	Field	3.78E10	9	1.70E-4	2.38E-4	3.31E-4
	G_F			8.50E-4	1.19E-4	1.56E-4
30	Field	2.7E11	108	3.7E-4	4.0E-4	4.4E-4
	G_F			1.8E-4	2.0E-4	2.2E-4
65	Field	4.15E7	2	1.99E-2	4.82E-2	1.32E-2
	A_I			4.97E-2	1.21E-2	3.32E-2
125	Test	1.08E9	10	6.75E-3	9.26E-3	1.26E-2
150	Test	1.16E9	7	4.08E-3	6.03E-3	8.82E-3
200	Test	4.66E8	2	1.76E-3	4.29E-3	9.18E-3
250	Test	6.64E7	3	2.31E-2	4.52E-2	8.31E-2
300	Test	3.11E7	4	7.39E-2	1.29E-1	2.16E-1
350	Test	2.07E7	8	2.69E-1	3.88E-1	5.50E-1

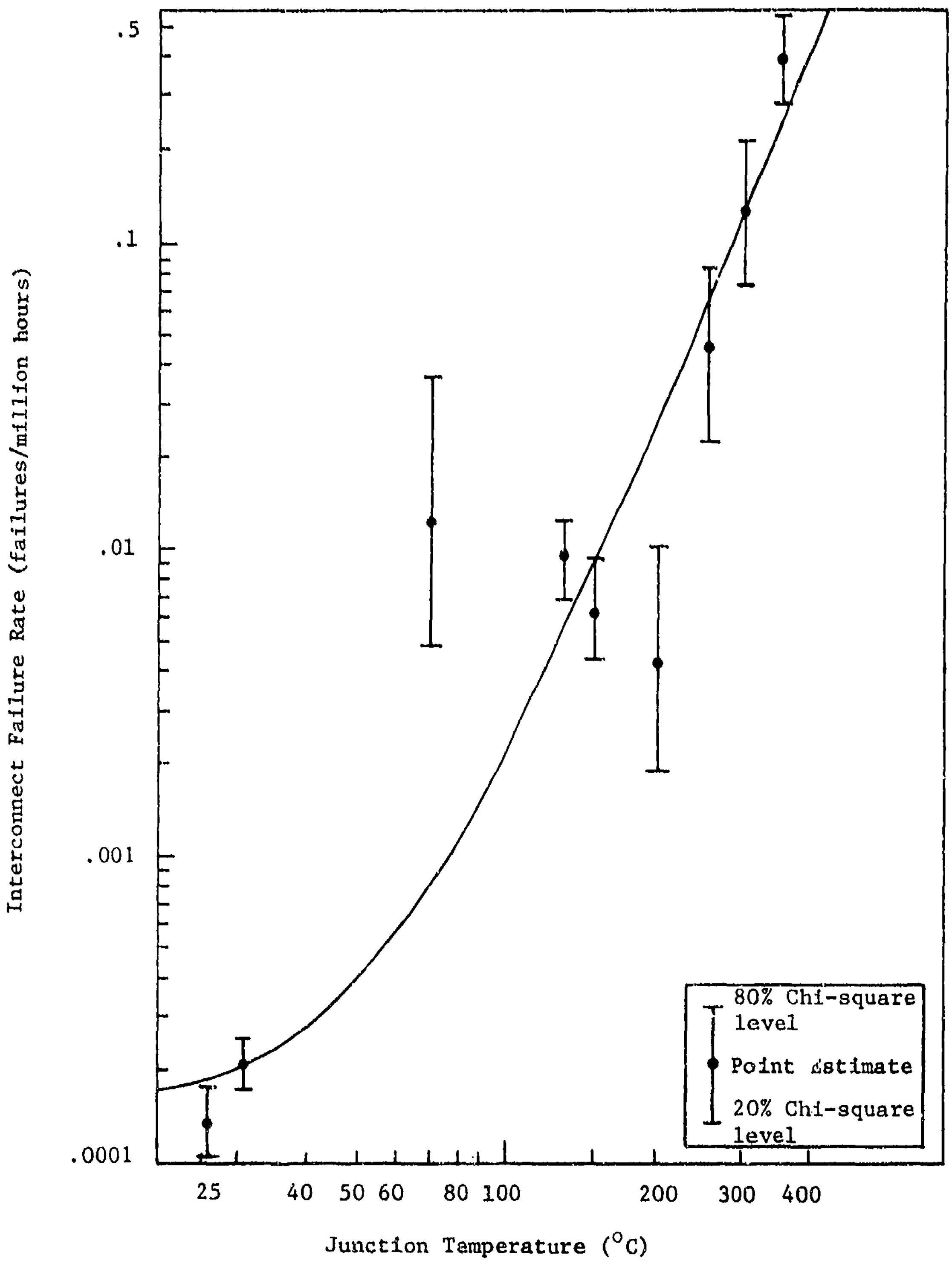


Figure 6: Single Metal and Solder Interconnection Failure Rates

failures, and die related failures. The results showed that 40% of the digital devices with less than 400 gates, memories with less than 4000 bits and all linear IC failures were attributable to package or interconnection failures. This percentage reduced to 20% for ICs with greater than 400 gates and memories of 4000 or more bits. This leads to die correction factors for the above categories of 0.6 and 0.8 respectively (Table 4).

To calculate a predicted failure rate for an integrated circuit using the model in Section 2.1 of MIL-HDBK-217B, it is necessary to know the operating temperature, application environment and temperature factors modifying unique parts of the prediction equation; they can not be simply "factored out" of the equation. Thus, these terms must be considered for each IC die.

An IC die used within a hybrid microcircuit will be subjected to essentially the same environment as a discretely packaged IC die under the same conditions. Thus, the environmental term used in the IC model should be the factor corresponding to the environment expected for the hybrid microcircuit.

The temperature factor in the monolithic model is based on the junction temperature of the IC. Within a hybrid microcircuit, the junction temperature may vary for each device within the package. The true junction temperature for each die can only be found by IR measurement (MIL-STD-883, Method 1012) or calculation if the θ_{JA} is known for each die. As this information is rarely available and requires special equipment and experience, this value can often only be estimated. The present model in MIL-HDBK-217B for discrete integrated circuits estimates a worst case junction to ambient temperature rise to be either 5, 10, 13 or 25°C, depending on the complexity and technology of the device. Extending this approximation to dice used within hybrid microcircuits is a simple yet reasonable solution to the problem of unknown junction temperatures.

IC dice are rarely available screened to any of the quality classifications presented in the IC model. Therefore, one quality classification should be assumed for all ICs. The choice of this factor is somewhat arbitrary, being important only in achieving the correct relative contribution when compared to the contributions of the other components to the base failure rate. As the overall hybrid quality factors will be normalized to Method 5008 or Method 5004, Class B of MIL-STD-883, a quality factor of 2.0 (Class B) was chosen.

4.3 Discrete Semiconductors

Though discrete semiconductors (transistors and diodes) are considerably less complicated than integrated circuits, their reliability may vary over a wide range due to the different voltage and power stress levels which they experience. Again the models given in MIL-HDBK-217B (Section 2.2) should be used to compute the contributions of semiconductor dice to the base failure rate of the hybrid.

While analyzing the failure analysis reports for discrete transistors, it was found that 60% of the reported failures were caused by package or interconnection failures. The data collected from failed diodes revealed that 80% of all reported failures were caused by package or interconnection failures. This indicates that the failure rates calculated by the discrete transistor or diode models must be multiplied by factors of 0.4 or 0.2 respectively to arrive at die failure rates which can be used in the hybrid microcircuit model.

The environmental factors given in the MIL-HDBK-217B semiconductor model were again adopted.

The power rating for a semiconductor die will be very dependent on the hybrid packaging. If studies have not been performed to determine the maximum power which can be safely dissipated, the power rating for the die discretely packaged will provide an estimate of this value. If the die is available in more than one discrete hermetic package, the worst case, or lowest rating, should be assumed.

When preliminary calculations were performed with the new model for devices for which a field failure rate was known, it was found that devices containing predominantly discrete semiconductors as opposed to maily IC's predicted a failure rate consistently higher than the experienced rate unless a quality factor corresponding to a JANTXV level was assumed for the discrete chips.

4.4 Capacitors

Ceramic chip capacitors are the most common type of capacitor used within hybrid microcircuits. As these devices are constructed the same as discrete ceramic capacitors, the model for these devices found in MIL-HDBK-217B may be adapted for chip capacitors used in hybrids. As military grade hybrids are rated to 125°C, the capacitors must be rated to 125°C.

Tantalum chip capacitors are also used in hybrids; again the same arguments apply as for the ceramic chip capacitors. The appropriate model from Section 2.6 of MIL-HDBK-217B is applicable to essentially all types of capacitors.

It was found that only 20% of discrete capacitor failures were due to lead failures, thus indicating a chip correction factor of 0.8.

A model quality classification of level M was found to give the best match to the chip capacitor data obtained from field data for which all failures were analyzed. Again, the application environment and temperature terms from the model should be used.

Table 4: Discrete Component to Die Failure Rate Correction Factors

Component	Correction Factor
Integrated Circuit	0.6 applied for digital devices of $\leq$ 400 gates, memories of $\leq$ 4000 bits, and all linear devices 0.8 applies for all digital devices of $\geq$400 gates and memories of $\geq$4000 bits
Transistors	0.4
Diodes	0.2
Capacitors	0.8

4.5 Film Resistors

Film resistors used in hybrid microcircuits may be thin or thick film, laid directly on the substrate or on chips which are later attached to the substrate. Film resistors have been shown to be very reliable. In fact, their contribution is negligible for most applications. IBM reported 90 billion thick film resistor operating hours with no failures (Ref. 6). Other data sources reported zero failures in 78 million hours and 8 failures in 6.0 billion hours. The last report was for non-screened and non-hermetic parts and showed 7 failures in the first 1.5 billion part hours and only one failure in the remaining 4.5 billion hours. Using the Chi-square tables, the failure rate for the IBM data can be shown to be less than 0.00002 failures per million hours at an 80% confidence level. The reported 78 million hours with zero failures would appear relatively inconsequencial compared to the other data. If the initial infant mortality failures from the last report are ignored and the last reporting period is considered to represent the inherent reliability of this part, the resulting point estimate failure rate would be 0.0002 failures per million hours. Since this was a non-hermetic device, this point estimate should be divided by 2 (see Section 5.1), thus giving a point estimate of 0.0001. As both data reports were from ground fixed systems operating at 25 to 30^{o}C, the failure rate term for a film resistor was selected to be the conservative estimate of 0.0001 (failures/million hours).

The failure mechanisms associated with film resistors, i.e. corrosion, conductor interface diffusion and parametric drift are generally temperature dependent. Therefore, the failure rate of a resistor should also be a function of temperature. There was not, however, sufficient data on these devices to derive such a relationship. For this reason, the film resistor failure rate dependence was estimated to be the same as that for a discrete film resistor as given in MIL-HDBK-217B, Section 2.5.2. The dependence was not found to be very extreme, hence this relationship was quantified into a table establishing the failure rate for discrete ranges of temperatures.

4.6 Hybrid Microcircuit Package

Hybrid microcircuit packages are designed to protect the circuit from contaminants such as moisture and stray particles as well as from mechanical damage. The failure analysis reports collected attributed nearly 10% of the reported failures to package problems. Of these, all but one was due to a leak in the seal. For this reason, it would seem reasonable to make the failure contribution of the hybrid's package a function of the package seal. The most important package seal attribute is the seal length. Other factors would seem to be package and seal material, temperature and application environment.

The effect of the various mechanical (environmental) stresses may be seen in Table 5 (Ref. 7). Constant acceleration tests seem to be especially damaging to the package. As there was not sufficient data to generate empirical environmental factors, the development of these factors will be discussed in Section 4.6.

Table 5: LEAK TEST RESULTS OF PACKAGES WHICH WERE ENVIRONMENTALLY CONDITIONED (Ref. 7)

Package Type	Method of Sealing	Seal or Reseal	Sample Size	Temperature Storage (150°C/100 Hr)	Temperature Cycling	Number of Package Failing Environmental Tests						Comments
						Moisture	Acceleration	Vibration	Thermal Shock	Altitude	Total Percent Failures	
Metal-Ceramic Flat-Pack	Manual Solder	Seal	7	0	0	0	0	0	0	0	0	
		Reseal	4	0	0		0	0	0	0	0	
	Peripheral Solder	Seal	4	0	0	0	1	0	0	0	25	The base of this package cracked at 10,000g
	Seam Solder	Seal	8	0	0	0	0	0	0	0	0	
Metal-Glass Flat-Pack	Thermal Conductivity Solder	Seal	16	0	0	0	2	0	0	0	12.5	The base of one of the packages came off during 10,000g The other package leaked at the cover
	Seam Solder	Seal	8	0	0	0	0	0	0	0	0	
Metal Flat Pack	Seam Seam Solder	Reseal	1	0	0	0	0	0	0	0	0	
	Peripheral Solder	Seal	9	0	0	0	0	0	1	0	11.1	The leak was at the cover seal
	Seam, Solder Solder	Seal	4	0	0	0	0	0	0	0		
	Seam Solder	Reseal	1	0	0	0	0	0	0	0		
	Seam Weld	Seal	7	0	0	0	0	0	0	0		
	Seam Weld	Reseal	4	0	0	0	0	0	0	0		
Metal-Ceramic Flat-Pack	Peripheral Solder	Seal	3	0	0	0	0	0	0	0		
	Seam Solder	Seal	2	0	0	0	0	0	0	0		
Metal Platform Packages	Peripheral Solder	Seal	11	1	0	0	2	0	[illegible]	1	45.5	All 7 packages failing leaked at the pins
	Seam Solder	Seal	7	0	0	0	1	0	0	0	14.3	
	Seam Solder	Reseal	1	0	0	0	0	0	0	0	0	
	Seam Weld	Seal	7	0	0	0	0	0	1	0	14.3	
	Seam Weld	Reseal	2	0	0	0	1	0	0	0	50.0	

Table 5 indicates that, with the exception of the metal platform package, no generalizations as to the relative reliability of any package or seal method could be drawn. The problem with the metal platform package was a thermal mismatch between the metal package and the glass seal around the leads and was limited to one manufacturer.

It was thought at the beginning of this study that any package factor would have to be dependent on the package type. Upon studying the problem closer, however, it became apparent that this might not be possible. There is a myriad of seal and package combinations with more being developed all the time. The aforementioned study (Ref. 7) concluded that it is very important that the package seal and lid chosen be carefully matched. The circuit to be enclosed within the package may impose additional constraints that could affect th relative reliability of the various package/seal combinations. Even the manufacturer of a particular package type has been shown to be significant in some instances.

Obviously, all these parameters cannot be considered by this model. However, if tests are performed to weed out substandard combinations, very little variation in the ability to withstand the given stresses will be observed as illustrated in Table 5. Just as the integrated circuit factor assumes that the given component will not be driven by voltage and power levels beyond those for which it was designed, so the package factor must assume that an intelligent choice was made when the package and seal method were specified. This assumption can be checked with the package qualification procedures found in MIL-STD-883, Method 5008 or 5004.

The package factor will then be only a function of seal length, temperature and application environment. Data collected from field data and life test data for which all failures were analyzed were used to develop an equation relating temperature and seal perimeter. The equation fit to this data is as follows:

$$\lambda_s = 0.011\ S\ [1-\exp(-S^2/50)]\ \exp\left[-5203\left(\frac{1}{T+273} - \frac{1}{298}\right)\right]$$

T = Hybrid Package Temperature (°C)

S = Seal Perimeter (Inches)

4.7 Environmental Factors for Film Resistors, Packages, and Interconnections

The models in MIL-HDBK-217B which can be adapted for components within a hybrid microcircuit quantify the effect of various environments on the component. There are, however, film (substrate) resistors, packages or interconnections. The data on the failure rates of these components did not cover the range of environments generally specified in the failure rate models, thus individual environmental modifiers could not be determined for these components. For this reason, as well as for simplicity, it was decided to use only one set of environmental factors for all the film resistors, interconnects, and package types. The wide variation in stress levels that may be encountered by a part within each general environmental classification makes the environmental factors rather broad and generalized to begin with, thus this assumption should not significantly reduce the accuracy of the overall environmental contribution.

The majority of hybrid field data collected for this study came from one of three environments: Airborne Inhabited, Airborne Uninhabited or Ground Fixed. To arrive at environmental factors, the data was divided into 12 groups of hybrid microcircuits of similar construction. Since the data entries would be combined with other entries before any analysis was performed, even the devices reporting no failures over the period of their field operation were included in this analysis.

The similar construction groups were then divided by operating environment. Average failure rates were calculated for each environment represented in each construction group and the ratios between these failure rates were tabulated. The environmental ratios were then averaged for all the construction groups (see Table 6). The ratio of the Airborne Uninhabited failure rates to the Airborne Inhabited failure rates was found to be 1.7 and the ratio between Airborne Uninhabited to Ground Fixed to be 3.4. There were only two groups with enough data from both Airborne Inhabited and Ground Fixed environments to derive a failure rate ratio between these two environments. As quite a large variance from the mean was noticed among the environmental ratios for the similar construction groups, this was not considered to be sufficient to establish a ratio between these environments with any confidence. However, knowing the ratios between the other two combinations, a ratio of 2.0 was derived for an Airborne Inhabited environment compared to a Ground Fixed environment.

The above are the ratio between the overall failure rates of a hybrid microcircuit in one environment compared to its failure rate in another environment. It is not necessarily the ratio of the failure rates of the film resistors, interconnections and package. The dependence of the active components on the environment has already been tabulated. The interaction of the environmental factors for the active components and for the film resistors, interconnects and package will determine the overall predicted effect of the environment on the hybrid. It was found, however, that the environmental ratios for the active components were very close to the ratios found for the overall hybrids. The discrete semiconductor models give environmental factors of 5.0, 25 and 40 for Ground Fixed, Airborne Inhabited and Airborne Uninhabited respectively. This gives a ratio of 1.6 for Airborne Uninhabited compared to Airborne Inhabited, which is very close to the ratio found for the hybrid microcircuits (1.7). The ratio in the discrete integrated circuit model is only partially dependent on the environmental factors; the integrated prediction will show a ratio somewhat lower than this. However, for small devices (SSI, MSI) and common temperatures (25°C to 65°C), the predicted failure ratio between these two environments should be very close to the ratio between the environmental factors.

As the ratio of Airborne Uninhabited to Airborne Inhabited failure rates appears to be approximately the same for the total hybrid microcircuit and for the active components, the same ratio is assumed for the film resistors, packages and interconnections.

Table 6: AVERAGE FAILURE RATES AND ENVIRONMENTAL RATIOS FOR THE DATA GROUPED BY CONSTRUCTION

Group	Ground Fixed Failure Rate *	Airborne Inhabited Failure Rate*	Airborne Uninhabited Failure Rate*	Ratio AU to AI	Ratio AU to GF
A	NA	10.1	NA	NA	NA
B	NA	5.94	23.4	3.94	NA
C	NA	8.33	37.2	4.47	NA
D	NA	27.4	35.0	1.28	NA
E	1.54	NA	5.37	NA	3.49
F	4.88	15.6	28.7	1.84	5.88
G	NA	50.0	73.5	1.47	NA
H	NA	2.47	1.15	0.466	NA
I	NA	10.9	7.18	0.659	NA
J	NA	36.2	50.0	1.38	NA
K	7.17	16.0	5.75	0.359	0.802
L	NA	50.0	50.0	1.00	NA
Average				1.69	3.39

* Failures/million hours

Hybrid microcircuits were found to exhibit a failure rate ratio of 3.4 for microcircuits used in an Airborne Uninhabited environment compared to those used in a Ground Fixed environment. Active devices used within the hybrid, however, predict more extreme ratios: 6 for the integrated circuit factors, and 8 for discrete semiconductors. This indicates that the environmental ratio (Airborne Uninhabited vs. Ground Fixed) for the other components within the hybrid must be less than the 3.4 for the total hybrid. Since approximately 21% of the hybrid failures are due to active component failures (see Fig. 2) and assuming an average active component environmental ratio of 6 to 1, this environmental ratio for the other components within the hybrid may be calculated to be approximately 2.7 (see below).

$$\begin{aligned} R(.79) + 6\ (.21) &= 3.4 \\ R &= 2.7 \end{aligned} \tag{4.7.1}$$

Therefore the ratios Airborne Uninhabited to Airborne Inhabited and Airborne Uninhabited to Ground Fixed for the film resistors, interconnects and package failure rate factors within the hybrid model were found to be 1.7 and 2.7 respectively. These ratios may be used to generate environmental factors of approximately 1, 2 and 3 for Ground Fixed, Airborne Inhabited and Airborne Uninhabited environments respectively.

There was not enough data to calculate ratios for the other environments; however, looking at the various discrete device models in MIL-HDBK-217B, it was found that Ground Mobile and Naval Sheltered environments often are assigned factors equal to those for an Airborne Inhabited environment, and that Naval Unsheltered environments are often given the same factors as those for Airborne Uninhabited environments. Since no evidence was available to warrant a change, this convention was retained for the new hybrid model.

Due to the very small amount of data available from Ground Benign, Space Flight and Missile Launch environments, factors of 0.2, 0.2 and 5.5 respectively were adopted for these environments. These values were selected from the monolithic model in MIL-HDBK-217B.

4.8 Die Attach Method

The method of attaching the components to the substrate may have a large effect on the reliability of a device. Recent studies by Sommerville and Traeger (Ref. 2 and Ref. 3) have shown that organic die attach materials outgas harmful products which may drastically reduce the reliability of a microcircuit. While organic die attachments which do not affect the reliability are possible, these studies have shown that the normal processing and vendor specified cure times are not sufficient to insure a reliable part.

Table 7: ENVIRONMENTAL FACTORS (Π_E) FOR PASSIVE COMPONENTS, INTERCONNECTIONS AND PACKAGES

Application Environment*	Symbol	Π_E
Ground Benign	G_B	0.2
Space Flight	S_F	0.2
Ground Fixed	G_F	1.0
Airborne Inhabited	A_I	2.0
Naval, Sheltered	N_S	2.0
Ground, Mobile	G_M	2.0
Airborne, Uninhabited	A_U	3.0
Naval Unsheltered	N_U	3.0
Satellite or Missile Launch	M_L	5.5

* Definitions of these environments are given in Table 2-3 of MIL-HDBK-217B

Water is the main contaminant outgassed. A new revision to MIL-STD-883, released 31 August 1977, specifies that all hybrid microcircuits must demonstrate an internal moisture content of less than 6000 ppm. In order to meet this specification, manufacturers using organic die attach methods must take special precautions to insure that the material used does not outgas extensively. Parts procured to MIL-STD-883B using organic die attach methods should then be nearly as reliable as microcircuits using eutectic attachments. The added reliability risk involved with using organic attachments in microcircuits for which no attempt is made to control outgassing should be accounted for by the quality factors.

Aside from the problem of outgassing from organic die attach materials, component attach failures were not found to be a significant cause of failure by either the RAC or Hughes field failure mechanism study. As no unique hybrid failure mechanisms associated with die bonds were found, component attach failures were considered to be adequately covered by the individual component failure rate contributions. Thus, no "component attach" term was included in the new hybrid model.

4.9 Substrate Metallization

There is a wide variety of substrate metallization materials and combinations of materials available to the hybrid designer. Several of these have been shown to be inherently unreliable. Others have been shown to be unreliable under certain conditions or when used in conjunction with some other material. It is beyond the scope of this model to attempt a detailed evaluation of every possible material. There are, however, several failure mechanisms which will affect most materials. Lack of adhesion to the substrate, cracks, corrosion caused by various contaminants, and shorts caused by particles are the most prevalent of these mechanisms. Lack of adhesion to the substrate and cracks in the metallization have been found to be yield problems and no examples of these failures were found in either the Hughes study (Ref. 1) or the RAC study of field failure modes (Section 3.3). It would appear that these problems have been removed by the initial testing and screening of the devices. Contamination of the substrate metallization may be caused by contaminants either sealed within the package (moisture, Cl from the lubricant used when drawing the internal wires, outgassing from epoxy, etc.) or allowed into the package through a leak in the seal. Failures caused by the latter will be considered by the package factor in the model. Failures caused by internal contaminants in theory, should not be a problem in a controlled system. Unfortunately, experience has shown otherwise. Particle induced shorts are about the same in this respect. To account for these failures, it is then necessary to quantify the metallization. "Length of metallization" is difficult to determine and simple "substrate area" does not necessarily give a good indication of the susceptibility of a device to corrosion or particles. Density would consider line spacing, thus the size of a particle or droplet which could cause failure, as well as giving a good indication of the amount of processing a given area had received. Development of this term is left to Section 4.11.

There is then no need for a separate "metallization" term. Rather, its contribution will be considered by the factors for the package (contamination allowed through the seal), or for the density.

4.10 Quality Factors

Most of the data obtained from hybrid microcircuits fell into the general classification of vendor equivalent to MIL-STD-883, Method 5004, Class B. Since Method 5008 has been just recently released, no data were available on parts procured to that specification. A qualitative analysis of the added features incorporated into Method 5008, however, gives a good idea of the relative reliability of parts screened to this level.

Method 5008 to MIL-STD-833B contains several new screens and quality assurance tests including moisture analysis, particle impact noise test, D.C. electrical measurements of all active semiconductor and integrated circuit chips, a bond strength test and a die shear test. These tests are specifically aimed at the major causes of failure for hybrid microcircuits. While most of these tests are not 100%, they should "weed out" any recurring process deficiencies. Approximately 75% of the failure analysis reports attributed the cause of failure to errors in the processing of the device rather than to excessive environmental stress or wear-out/chemical reactions such as external corrosion but not including corrosion caused by excessive moisture sealed within the package. Many of these failures could have been eliminated if the part had been screened to Method 5008. While a significant percentage of these parts may have been random failures and thus slipped through the sampling screens, the effect of this screening procedure should still be significant.

Although the true effect of screening to MIL-STD-883, Method 5008 cannot be accurately evaluated until parts screened to this procedure are actually operated in the field, it is estimated that these parts should exhibit a failure rate equal to approximately one quarter that of parts screened to a vendor equivalent of Method 5004, Class B.

The "commercial" classification covers a very broad range of materials, process controls and screening requirements. The hybrid microcircuit market is especially broad. Very little industry standardization is noticeable outside of the military grade devices. Hybrids have been made using a myriad of materials; substrate metallization from gold to copper, packages from a thin plastic coating to metal-ceramic flat packs, interconnections from thermocompression bonded gold wire to silver filled epoxy. For virtually every step in the complex hybrid assembly process there exists a multiplicity of means of implementing that step. Screening requirements as well as inprocess quality assurance practices of the various manufacturers also vary widely from the manufacturer who qualifies all equipment for each lot followed by a complete screening program to one who gives only a final parametric test. It is, therefore, nearly impossible to create enough categories to accurately consider even the more significant process or material variations. As MIL-HDBK-217B is primarily concerned with procurement of parts for generally high reliability military systems, the factor given for the commercial classification should predict a value somewhat pessimistic of what is considered an

average commercial reliability. This provides a margin of error to guard against a poor design or process which would otherwise be identified by the screening requirements of the higher quality grades. Therefore, the hybrid commercial quality factor was established as being 60 times greater than the Class B (Method 5004) or Method 5008 part.

Certain applications place a very high premium on reliability. Parts used in such cases may be purchased to a tighter specification than found in MIL-STD-883 and MIL-M-38510. These parts should indeed display a longer mean life-time and thus there should be a term in the model to reflect this effect. Currently, however, there is no standard specification to define this higher quality level. Work on a specification for a "Class S" hybrid microcircuit is being coordinated by RADC; however, results are not expected for several months.

A definition of these quality levels and their respective factors are given in Table 8.

4.11 Circuit Function Factor

The models within MIL-HDBK-217B for integrated circuits and semiconductors contain a term which is dependent upon the function of the circuit, whether it is linear or digital. Such a term will account for the higher voltages, higher temperatures and tighter tolerances on parameter drift which may be encountered in linear devices. To account for the effect of such conditions on the chip or substrate resistors, interconnections and package, a term modifying the factors for these components was introduced during the final fit of the model to the field data. The best fit to the data was obtained with a value of 1.25 assigned for all linear and linear-digital combination circuits and 1.0 for all digital circuits.

4.12 Density Factor

After the form of the base failure rate for this model had been determined a multiple linear regression program was run to arrive at the best fit to the data. The residuals for this regression are shown in Table 9. The resultant r^2 (multiple correlation coefficient) indicated that only 42% of the variance in the data was explained by the model. It would appear that there must be some other variable(s) which would explain a large part of this variation. It was hypothesized that a density term could explain some of this variation. A more dense microcircuit will require a tighter tolerance on several manufacturing steps, such as wire bonding, and will necessitate closer spacing of interconnect wires and substrate metallization lines. Closer lines make the circuit more susceptible to electrochemical corrosion and can be shorted by smaller particles. Additionally, each manufacturing step may be viewed as a possible source of contaminants; as such, the more processing each square inch of substrate receives, the higher the probability of failure.

Table 8: QUALITY FACTORS (Π_Q)

Quality Level	Description	Π_Q
S	The test procedures for this quality level are currently being developed. Until such time that they are included in MIL-STD-883 and MIL-M-38510, the procuring activity will provide the necessary testing requirements and Π_Q value	
B	Procured to the Class B requirements of: MIL-STD-883, Method 5008 and Appendix G of MIL-M-38510 or MIL-STD-883, Methods 5004 and 5005 and MIL-M-38510	1.0
D	Commercial part, hermetically sealed, with no screening beyond manufacturer's normal quality assurance practices	60.0

Table 9: RESIDUALS FROM THE STEPWISE MULTIPLE LINEAR REGRESSION FIT OF THE BASE FAILURE RATE TO THE FIELD FAILURE RATE

OBS	Y-OBS	Y-CALC	ERROR	%-ERR	C-ER^2
1	1.5385	4.2718	-2.7333	-63.99	7.4712
2	3.8462	3.0288	0.8174	26.99	8.1393
3	9.2308	6.4154	2.8154	43.89	16.0658
4	1.0526	4.1266	-3.0740	-74.49	25.5153
5	1.0000	2.2870	-1.2870	-56.28	27.1717
6	4.7619	4.0450	0.7169	17.72	27.6857
7	23.0769	13.7261	9.3508	68.12	115.1229
8	50.0000	23.8882	26.1118	109.31	796.9498
9	52.6316	34.2952	18.3364	53.47	1133.1723
10	17.5000	22.1461	-4.6461	-20.98	1154.7588
11	9.3023	14.4452	-5.1429	-35.60	1181.2079
12	13.8889	46.4057	-32.5168	-70.07	2238.5532
13	18.1818	29.7450	-11.5632	-38.87	2372.2597
14	1.6667	18.9251	-17.2584	-91.19	2670.1137
15	2.5000	10.4280	-7.9280	-76.03	2732.9670
16	78.9474	37.8315	41.1159	108.68	4423.4808
17	14.2857	11.2809	3.0048	26.64	4432.5098
18	7.6923	27.5447	-19.8524	-72.07	4826.6275
19	0.2778	4.7618	-4.4840	-94.17	4846.7336
20	2.1053	4.4476	-2.3423	-52.67	4852.2201
21	7.6923	4.9342	2.7582	55.90	4859.8275
22	6.1538	4.9977	1.1562	23.13	4861.1642
23	6.1538	4.8979	1.2560	25.64	4862.7418
24	10.7692	4.9432	5.8260	117.86	4896.6841
25	3.0769	5.1247	-2.0478	-39.96	4900.8774
26	3.4286	5.7417	-2.3131	-40.29	4906.2279
27	5.1724	5.4513	-0.2789	-5.12	4906.3057
28	7.3913	5.6509	1.7404	30.80	4909.3346
29	3.4483	3.9905	-0.5423	-13.59	4909.6287
30	9.2308	3.8907	5.3400	137.25	4938.1447
31	0.2214	2.5570	-2.3355	-91.34	4943.5994

C-ER ^ 2 = Cummulative Error Squared

As density describes the entire microcircuit rather than being a component within the microcircuit, its effect will be seen as the increased failure rate of the components within the hybrid. Thus, the density term should multiply the base failure rate rather than be an additive term.

Accepting these arguments, the next step was to define density. Power dissipated per square inch of substrate would influence the temperature of the device but would have little correlation with such things as line spacing and manufacturing tolerances. Power dissipation would also be a rather complicated calculation for some hybrid microcircuits. Attached components per square inch of substrate is simple calculation and should be correlated with the above considerations.

Analyzing the fit to the data obtained using attached components per square inch as the definition of density, revealed that predictions for circuits which employed mainly transistors and diodes (as opposed to those containing mainly integrated circuits) were consistently higher than the failure rates found in the data.

In an attempt to remove this effect, density was redefined as the number of interconnections per square inch of substrate. In this way, integrated circuits were weighted more than discrete semiconductors. The fit to the data using this definition eliminated the bias on discrete semiconductors; however, it was found that the very small devices (substrate area less than 0.2 square inches) now had predicted failure rates consistently higher than the failure rates reported from the field.

To correct this inaccuracy, density was again redefined. A constant term was added to the substrate area to straighten the density curve in the region for small devices.

The final acceptable fit to the data was obtained using the following definition:

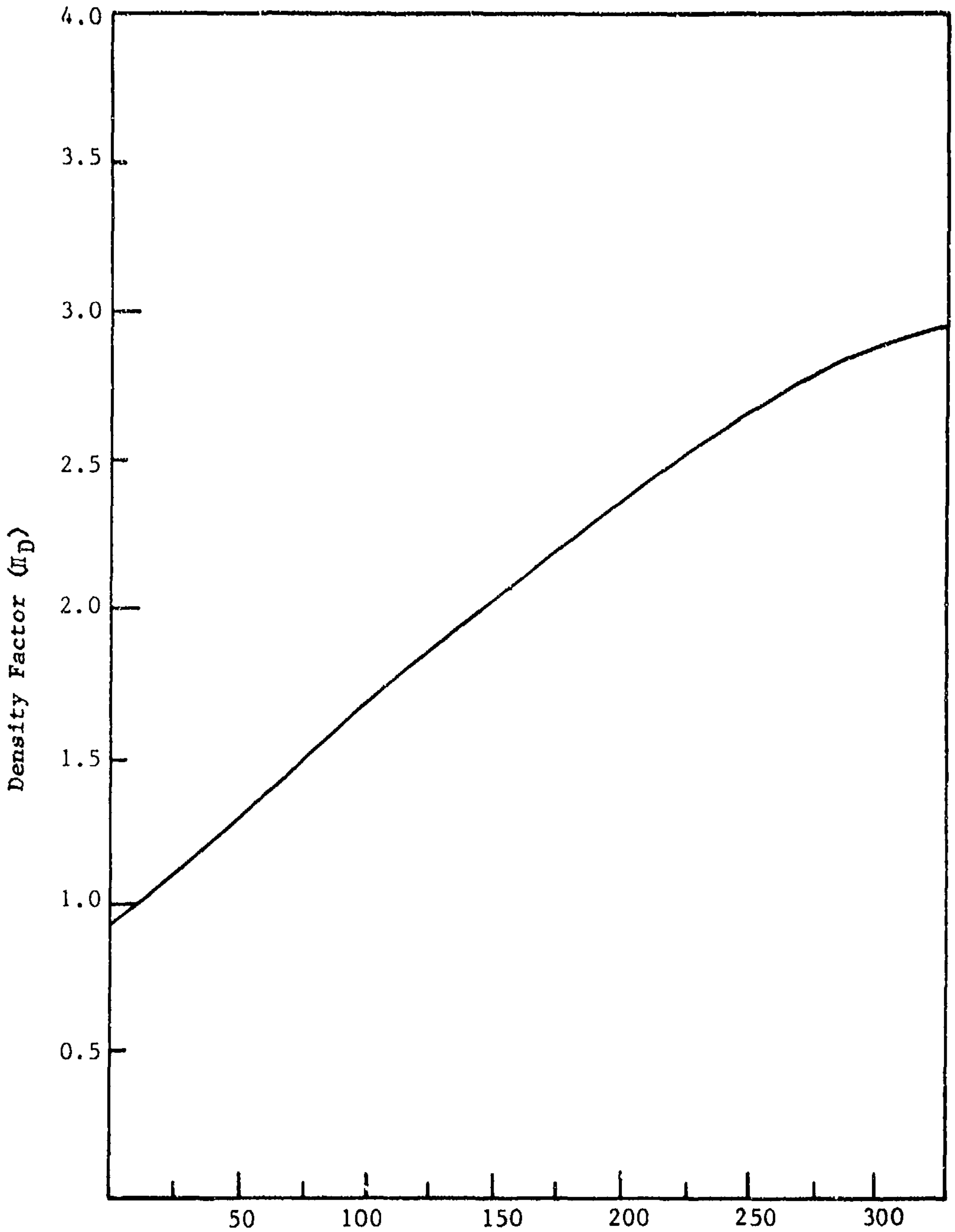
$$\text{Density} = \frac{\text{number of interconnections}}{(A_s + 0.10)} \qquad (4.12.1)$$

A_s = substrate area (square inches)

The best fit to the data was obtained with the density term (Π_D) the result of the following function:

$$\Pi_D = 0.2 + 0.15(\sqrt{\text{Density}}) \qquad (4.12.2)$$

This function describes the typical "S" shaped curve shown in Figure 7.



$$\text{Density} = \frac{\text{No. of Interconnections}}{\text{Substrate Area} + 0.10}$$

Figure 7: Density Factor (Π_D)

Section V

ADAPTATIONS FOR SPECIAL APPLICATIONS

For every general procedure there is always a surprising number of exceptions. The most common exceptions and the corresponding adjustments are identified in this section.

5.1 Hermetic Packages Enclosing More Than One Substrate

Hybrid packages containing several substrates stacked together are not uncommon. The adjustments for this variation are relatively obvious. A base failure rate, density and function factor should be calculated for each substrate. The sum of these terms for each substrate should be multiplied by the device quality factor to arrive at the predicted failure rate. (Note: the package factor should only be included in the base failure rate for the substrate with the largest area. If two or more have equal areas, the substrate mounted on or serving as the package header should be used).

5.2 Multilevel Metallization

Multilevel metallization patterns were found to be quite reliable. No failures due to multilevel related construction were reported. In general, multilevel faults are weeded out during the screening and testing of the microcircuit. Thus no factor considering the number of levels was necessary. Multilevel microcircuits are often more dense than single level metallization microcircuits and thus less reliable in this respect. Several multilevel devices were considered when the density term was derived. The finished model showed a good fit to the data from the multilevel metallization devices.

Section VI

PROPOSED HYBRID MODEL

This section outlines the hybrid model as accepted by the government-industry coordination meeting held January 24-25 at Griffiss AFB. The format and paragraph numbering are consistent with MIL-HDBK-217B.

2.17 Hybrid Microcircuit

The hybrid failure rate model is:

$$\lambda_p = \{\Sigma N_C \lambda_C \Pi_G + [N_R \lambda_R + \Sigma N_I \lambda_I + \lambda_S] \Pi_F \Pi_E\} \Pi_Q \Pi_D$$

(failures/million hours)

where:

$\Sigma N_C \lambda_C \Pi_G$ is the sum of the adjusted failure rates for the active components and capacitors in the hybrid from Section 2.1.7.1.

N_C is the number of each particular component
λ_C is the component failure rate
Π_G is the die correction factor from Table 2.1.7-1.

$N_R \lambda_R$ is the number of (N_R) and failure rate contribution (λ_R) of the chip or substrate resistors (Section 2.1.7.2)

$\Sigma N_I \lambda_I$ is the sum of the failure rate contributions of the interconnections (λ_I) from Section 2.1.7.3

λ_S is the failure rate contribution of the hybrid package (Table 2.1.7-4)

Π_E is the environmental factor for the film resistors, interconnections and package from Table 2.1.7-5

Π_Q is the quality factor from Table 2.1.7-6

Π_D is the density factor from Table 2.1.7-7

Π_F is the circuit function factor

= 1.0 for digital hybrids
= 1.25 for linear or linear-digital combinations

2.1.7.1 The sum of the adjusted failure rates for the active components and capacitors shall be calculated as follows:

N_C is the number of each particular component

λ_C is the failure rate contribution for a particular component predicted using the correct model from the following sections in this handbook:

Integrated Circuits	Section 2.1
Discrete Semiconductors	Section 2.2
Packaged Resistors	Section 2.5
Capacitors	Section 2.6

When calculating λ_C, assume a quality factor corresponding to Quality Level B (integrated circuits), JANTXV (discrete semiconductors), or Level M, 125°C rating (capacitors). Use the environmental factor corresponding to the application environment of the hybrid, and assume a component ambient temperature equal to the temperature of the hybrid package.

If the maximum rated stress for a die is unknown, it shall be assumed to be the same as that for a discretely packaged die of the same type. If the same die has several ratings based on the discrete package type, the lower value will be assumed. Power rating used should be based on case temperature for discrete semiconductors.

π_G adjusts the calculated discrete component failure rate to a die or capacitor chip failure rate. For packaged components, $\pi_G = 1.0$.

Table 2.1.7-1. DIE AND CAPACITOR CHIP CORRECTION FACTORS

Component	Π_G
Integrated Circuit	0.6* 0.8*
Transistors	0.4
Diodes	0.2
Capacitor Chips	0.8

*0.6 applies to digital devices ≤400 gates, memories of <4000 bits and all linear devices

*0.8 applied to digital devices of >400 gates and memories ≥4000 bits

2.1.7.2 The failure rate contribution of the chip or substrate resistors used in the hybrid (either on chips or directly on the substrate) is calculated as the product:

$$N_R \quad \lambda_R$$

Where:

N_R is the number of chip or substrate resistors

λ_R is the failure rate of the chip or substrate resistors **as given in Table 2.1.7.2.**

Table 2.1.7-2: BASE FAILURE RATES FOR CHIP OR SUBSTRATE RESISTORS

0.00010	for $T \leq 50^{\circ}C$
0.00015	for $50 < T \leq 80^{\circ}C$
0.0002	for $80 < T \leq 100^{\circ}C$
0.00025	for $100 < T \leq 125^{\circ}C$
0.0003	for $125 < T \leq 150^{\circ}C$

Where T is the hybrid package temperature

2.1.7.3 The failure contribution of the interconnections is the product:

$$N_I \; \lambda_I$$

Where:

N_I is the number of interconnections

λ_I is the temperature dependent failure rate for the interconnections from Table 2.1.7-3

Interconnections, as defined for this model are counted as one for every wire. Each beam lead or solder bump shall also be counted as one interconnection.

Only active (current carrying) interconnections shall be counted.

A bond is considered bimetallic if any one of the bond interfaces involves more than one type of metal.

Active die attach bonds (die to substrate bonds) are not counted as interconnections.

Redundant interconnections shall be counted as only one interconnection.

If an accurate count of the actual interconnections cannot be obtained, the following approximations may be made:

Component	Number of Interconnections
Each IC Chip Bonding Pad	1
Each Transistor	2
Each Diode	1
Each Capacitor	2
Each External Lead	1
Each Chip Resistor	2

HERMETIC PACKAGES ENCLOSING MORE THAN ONE SUBSTRATE

Each substrate shall be treated as a separate hybrid. Each substrate shall include its own density and function factor; however, only the largest substrate (area) or the substrate mounted on or serving as the package header (if all are of equal size) shall include a package factor. The hybrid failure rate will be the sum of the failure rates for the individual substrates.

MULTILAYERED METALLIZATION

The Model is valid for up to three layers of metallization.

2.1.7.3 Prediction Example for Hybrid Microcircuits

Microcircuit Description - Driver

Package: Hermetic Flatpack 1.15 x .95 in. seal, .75 x .75 in. substrate

Interconnections: 34 Gold-Aluminum, 4 solder

Active Components:

1 - LM106
1 - μA741
2 - Si NPN Transistor, 60% stress ratio (power and voltage), <1 watt
2 - Si PNP Transistor, 60% stress ratio (power and voltage), <1 watt
2 - Si General Purpose Diode, 60% stress ratio (power and voltage), small signal

Passive Components:

2 - Ceramic Chip Capacitors, 60% stress ratio
17 - Thick Film Resistors

Environment: Airborne Uninhabited, 65°C package temperature

Screened to MIL-STD-883, Method 5008, in accordance with Appendix G to MIL-M-38510

Example Calculations:

$$\lambda_p = \{\Sigma N_C \lambda_C \pi_G [N_R \lambda_R + \Sigma N_I \lambda_I + \lambda_S] \pi_F \pi_E\}\pi_Q \pi_D$$

Failure Rates for Components (λ_C)

LM106 die - 13 transistors - page 2.1.2-1

$1.0\ (2.0)\ [0.0039(5.0) + 0.0105(6.0)]\ 0.6 = 0.099$

µA741 die - 23 transistors - page 2.1.2-1

$1.0\ (2.0)\ [0.0061(5.0) + 0.014(6.0)]\ 0.6 = 0.137$

Si NPN transistor die, 60% stress ratio - page 2.2.1-1

$0.020(40)(1.5)(0.2)(1.0)0.88(1.0)0.4 = 0.084$

Si PNP transistor die, 60% stress ratio - page 2.2.1-1

$0.034(40)(1.5)0.2(1.0)(0.88)1.0(0.4) = 0.144$

Si General Purpose Diode die, 60% stress ratio - page 2.2.4-1

$0.0095(40)0.5(1.0)(1.0)0.7(1.0)0.2 = 0.0266$

Ceramic Chip Capacitor - page 2.6.1-1

$0.018(1.0)10(0.8) = 0.144$

Thick Film Resistor - Table 2.1.7-2

0.00015

Package - Table 2.1.7-4

$\lambda_S = 0.014$

Interconnections - Table 2.1.7-3

Au-Al: 0.00130

Solder: 0.000871

$\pi_E = 3.0$ Table 2.1.7-5

$\pi_Q = 1.0$ Table 2.1.7-6

Density = 38/(0.563 + 0.10) = 57.3

$\pi_D = 1.34$ Table 2.1.7-7

$\pi_F = 1.25$

$$\lambda_p = \{0.099 + 0.137 + 2\ (0.084) + 2(0.144) + 2(0.0266) + 2\ (0.144) + [0.00015(17) + 0.014 + 34\ (0.00131) + 4\ (0.00087)]\ (3.0)\ 1.25\}\ 1.0\ (1.34)$$

$$= \mathbf{1.71}$$

Table 2.1.7-3: INTERCONNECTIONS FAILURE RATE (λ_I)

Temperature (°C)*	λ_{I1}	λ_{I2}
25.	0.000174	0.000174
30.	0.000230	0.000218
35.	0.000302	0.000271
40.	0.000394	0.000334
45.	0.000508	0.000410
50.	0.000650	0.000499
55.	0.000826	0.000604
60.	0.00104	0.000727
65.	0.00130	0.000871
70.	0.00162	0.00103
75.	0.00201	0.00123
80.	0.00247	0.00145
85.	0.00302	0.00170
90.	0.00367	0.00199
95.	0.00444	0.00231
100.	0.00534	0.00268
105.	0.00639	0.00310
110.	0.00762	0.00356
115.	0.00904	0.00409
120.	0.0106	0.00467
125.	0.0125	0.00531
130.	0.0147	0.00603
135.	0.0171	0.00682
140.	0.0199	0.00770
145.	0.0231	0.00866
150.	0.0266	0.00971

λ_{I1} is for bimetal bonds (Gold-Aluminum)

λ_{I2} is for single metal bonds (Aluminum-Aluminum, Gold-Gold, etc) of solder

$$\lambda_{I1} = 0.000174 \exp\left[\left(-5075\right)\left(\frac{1}{T + 273} - \frac{1}{298}\right)\right] \text{ for } T \leq 150^\circ C$$

$$1.96 \times 10^{-6} \exp\left[\left(-9594\right)\left(\frac{1}{T+273} - \frac{1}{298}\right)\right] \text{ for } T > 150^\circ C$$

$$\lambda_{I2} = 0.000174 \exp\left[\left(-4056\right)\left(\frac{1}{T+273} - \frac{1}{298}\right)\right]$$

T = package temperature $(^\circ C)$

If metal system is unknown, assume worst case (λ_{I1})

* Hybrid Package Temperature

Table 2.1.7-4: PACKAGE FAILURE RATE (λ_S)

SEAL	25C / 70C	30C / 80C	35C / 90C	40C / 100C	45C / 110C	50C / 120C	55C / 130C	60C / 140C	65C / 150C
1.75	0.0011	0.0015	0.0020	0.0026	0.0034	0.0044	0.0056	0.0072	0.0090
	0.0113	0.0174	0.0261	0.0383	0.0551	0.0778	0.1081	0.1478	0.1990
2.00	0.0017	0.0023	0.0030	0.0039	0.0051	0.0065	0.0084	0.0106	0.0134
	0.0167	0.0257	0.0385	0.0566	0.0815	0.1151	0.1599	0.2186	0.2944
2.25	0.0024	0.0032	0.0042	0.0055	0.0071	0.0092	0.0118	0.0149	0.0188
	0.0235	0.0362	0.0543	0.0798	0.1148	0.1622	0.2253	0.3079	0.4148
2.50	0.0032	0.0043	0.0057	0.0075	0.0097	0.0125	0.0160	0.0202	0.0255
	0.0319	0.0491	0.0736	0.1081	0.1556	0.2199	0.3054	0.4175	0.5624
2.75	0.0042	0.0057	0.0075	0.0098	0.0127	0.0164	0.0210	0.0266	0.0335
	0.0420	0.0645	0.0968	0.1421	0.2045	0.2890	0.4014	0.5487	0.7390
3.00	0.0054	0.0073	0.0096	0.0126	0.0163	0.0210	0.0268	0.0341	0.0429
	0.0537	0.0825	0.1239	0.1819	0.2618	0.3700	0.5138	0.7024	0.9461
3.25	0.0068	0.0091	0.0120	0.0157	0.0204	0.0263	0.0336	0.0427	0.0537
	0.0673	0.1034	0.1551	0.2278	0.3279	0.4633	0.6435	0.8797	1.1848
3.50	0.0084	0.0112	0.0147	0.0193	0.0251	0.0323	0.0413	0.0524	0.0660
	0.0827	0.1270	0.1906	0.2800	0.4030	0.5694	0.7908	1.0810	1.4560
3.75	0.0101	0.0135	0.0178	0.0233	0.0303	0.0391	0.0499	0.0634	0.0798
	0.0999	0.1536	0.2305	0.3384	0.4871	0.6883	0.9559	1.3067	1.7600
4.00	0.0120	0.0161	0.0212	0.0278	0.0361	0.0465	0.0595	0.0755	0.0951
	0.1191	0.1830	0.2746	0.4032	0.5804	0.8201	1.1390	1.5569	2.0971
4.50	0.0165	0.0220	0.0291	0.0381	0.0494	0.0637	0.0814	0.1033	0.1301
	0.1629	0.2503	0.3757	0.5517	0.7940	1.1219	1.5582	2.1300	2.8690
5.00	0.0216	0.0289	0.0381	0.0500	0.0649	0.0836	0.1069	0.1356	0.1708
	0.2138	0.3286	0.4932	0.7242	1.0424	1.4728	2.0456	2.7963	3.7663
5.50	0.0275	0.0366	0.0484	0.0634	0.0823	0.1061	0.1356	0.1721	0.2168
	0.2713	0.4170	0.6258	0.9191	1.3228	1.8691	2.5959	3.5485	4.7795
6.00	0.0339	0.0452	0.0597	0.0782	0.1016	0.1308	0.1673	0.2122	0.2674
	0.3347	0.5143	0.7720	1.1336	1.6317	2.3054	3.2020	4.3770	5.8954
6.50	0.0408	0.0544	0.0719	0.0942	0.1223	0.1575	0.2014	0.2555	0.3220
	0.4030	0.6193	0.9295	1.36[illegible]	1.9646	2.7759	3.8554	5.2702	7.0985
7.00	0.0481	0.0642	0.0848	0.1111	0.1442	0.1858	0.2375	0.3014	0.3797
	0.4753	0.7304	1.0962	1.6097	2.3170	3.2737	4.5468	6.2153	8.3714
7.50	0.0557	0.0743	0.0982	0.1286	0.1671	0.2152	0.2751	0.3491	0.4398
	0.5505	0.8460	1.2697	1.8646	2.6838	3.7920	5.2666	7.1993	9.6968
8.00	0.0635	0.0847	0.1120	0.1467	0.1905	0.2454	0.3137	0.3981	0.5016
	0.6277	0.9647	1.4478	2.1262	3.0603	4.3239	6.0055	8.2093	11.0572

$$\lambda_S = 0.011\ S \left[1 - \exp\left(-S^2/50\right) \right] \exp\left[-5203 \left(\frac{1}{T+273} - \frac{1}{298} \right) \right]$$

T = Package Temperature ($^{\circ}$C)

S = Seal Perimeter (inches)

Table 2.1.7-5: ENVIRONMENTAL FACTOR FOR RESISTORS, INTERCONNECTIONS AND PACKAGES

Environment	π_E
G_B	0.2
S_F	0.2
G_F	1.0
A_I	2.0
N_S	2.0
G_M	2.0
N_U	3.0
A_U	3.0
M_L	5.5

Table 2.1.7-6: QUALITY FACTORS (Π_Q)

Quality Level	Description	π_Q
S	The test procedures for this quality level are currently being developed. Until such time that they are included in MIL-STD-883 and MIL-M-38510, the procuring activity will provide the necessary testing requirements and π_Q value.	
B	Procured to the Class B requirements of: MIL-STD-883, Method 5008 and Appendix G of MIL-M-38510 or MIL-STD-883, Methods 5004 and 5005 and MIL-M-38510.	1.0
D	Commercial Part, hermetically sealed, with no screening beyond manufacturer's normal quality assurance practices.	60.0

Table 2.1.7-7: DENSITY FACTOR (Π_D)

$$\text{Density} = \frac{\text{Number of Interconnections}}{(A_S + 0.10)}$$

A_S = area of substrate (squre inches)

$\pi_D = 0.2 + 0.15\ (\sqrt{\text{Density}})$

Density	Π_D	Density	Π_D
15.	0.78	160.	2.10
20.	0.87	165.	2.13
25.	0.95	170.	2.16
30.	1.02	175.	2.18
35.	1.09	180.	2.21
40.	1.15	185.	2.24
45.	1.21	190.	2.27
50.	1.26	195.	2.29
55.	1.31	200.	2.32
60.	1.36	205.	2.35
65.	1.41	210.	2.37
70.	1.45	215.	2.40
75.	1.50	220.	2.42
80.	1.54	225.	2.45
85.	1.[illegible]3	230.	2.47
90.	1.62	235.	2.50
95.	1.66	240.	2.52
100.	1.70	245.	2.55
105.	1.74	250.	2.57
110.	1.77	255.	2.60
115.	1.81	260.	2.62
120.	1.84	265.	2.64
125.	1.88	270.	2.66
130.	1.91	275.	2.69
135.	1.94	280.	2.71
140.	1.97	285.	2.73
145.	2.01	290.	2.75
150.	2.04	295.	2.78
155.	2.07	300.	2.80

Note - The density term is intended as a measure of the mechanical complexity of the hybrid as a whole.

Section VII

EVALUATION OF PROPOSED HYBRID MODEL

7.1 Comparison of Proposed Model to Field Experience

A comparison of the failure rate data to that predicted using the proposed model appears in Table 10 and is graphed in Fig. 8. The data is actual field experience for which there was at least 2 failures and at least 100,000 part hours reported. Data from laboratory tests or AGREE type (Reliability Demonstration) tests were not included. All data points listed are each from only one design (part number). None are combinations of data from different designs. The 60% interval is defined as the area between the 80% Chi-square level and the 20% Chi-square level. The diagonal line in Figure 8 represents that set of points for which the predicted value would exactly equal the experienced value. How close a data point is to this line indicates how good the prediction is at estimating the field performance. Comparing this graph to Figure 1 shows a definite improvement over the previous model. This new model shows a correlation coefficient of 0.913 with the field data.

To further check this model, predictions were calculated for all the devices for which the detailed part description was available. The relative contributions of the various components are indicated in Figure 9. If the failure analysis reports are divided into the same general categories, the pie chart in Figure 10 will result. For Figure 10, the contamination and particle induced shorts were not included, as they are not related to any one component, but rather to the size and process standards of the hybrid microcircuit as a whole. Comparing Figures 9 and 10 shows a very close correlation between the relative failure percentages.

7.2 Comparing the Proposed Model to an Equivalent Discrete Circuit

One of the deficiencies of the 20 September 1974 model was that it would predict the failure rate for a hybrid microcircuit which would be lower than the 217B prediction for an equivalent circuit constructed of discrete components in one environment, while predicting the discrete circuit to be substantially better in another environment (Example 1). As the new model follows the discrete predictions much more closely, one would not expect this problem with the new model. A recalculation of this example per the new model appears in Example 2. Example 1 indicates that the models predict a discrete circuit failure rate 2.5 times better than a hybrid in a Missile Launch application but 6.5 times worse in a Space Flight application. The new model predicts the hybrid to be a factor of 2.5 worse in a Missile Launch application and 1.4 times better in a Space Flight application. While the new model shows substantially less variation with environment, there is still a significant increase in the hybrid prediction compared to the increase of the discrete prediction. Analyzing the model reveals that the major reason for this increase is the contribution of the interconnections. Devices used in a Missile Launch environment will experience strong acceleration and vibrational stresses. The

discrete components used in the circuit calculated by the discrete model will probably contain Al wires bonded to the Al chip metallization. The hybrid microcircuit, however, contains gold wires bonded to the Al metallization on the components. Gold wires, being more dense, are much more susceptible to high acceleration stresses than are Al wires. Additionally, hybrids operated at very high temperatures such as these are, may be expected to form Au-Al intermetallic compounds which are generally brittle, thus making the bonds even more prone to failure under the mechanical stresses associated with the Missile Launch environment. The Al-Al bonds in the discrete devices should not experience this problem. The larger package and substrate involved in the hybrid will also be more likely to fail under the strong mechanical stress. Following this reasoning, it would appear that the hybrid microcircuit should indeed have a significantly higher failure rate than an equivalent discrete circuit in a Missile Launch environment.

Continuing the comparison of the hybrid to the discrete circuit, further calculations were made for another circuit (Example 3). This comparison assumed the discrete integrated circuits to be one of quality level B-1. The highest hybrid quality level corresponds to this discrete level as there are no military slash sheets for hybrid microcircuits at this time. For this example, the hybrid microcircuit model predicts a failure rate almost identical to that predicted for an equivalent discrete circuit.

Appendix D also shows predictions calculated for a wide range of circuits compared to predictions made for discrete components. These values are also compared to the prediction calculated using the MIL-HDBK-217B model.

Table 10: COMPARISON OF EXPERIENCED AND PREDICTED FAILURE RATES

(PER PROPOSED MODEL)

Hybrid Microcircuit	No. Fail.	Part Hour	Lower Limit*	Point Estimate*	Upper Limit*	New Prediction*
Temperature Control-Voltage Regulator	2	1.26E6	0.654	1.59	3.40	2.38
Delay Driver	12	1.32E6	6.84	9.09	12.0	9.07
Quad Logic Converter	4	3.80E6	0.604	1.05	1.77	1.89
Current Driver	38	3.84E7	0.853	0.990	1.15	1.04
Signal Processor (Class C)	8	3.95E5	14.1	20.3R 13.6A	28.8	34.6
12 Bit SSI Register	6	2.54E5	15.4	23.6R 13.6A	35.7	10.3
Dual Voltage Regulator (AU)	14	7.22E5	15.0	19.4R 12.4A	25.1	8.25
Dual Voltage Regulator (AI)	4	4.35E5	5.20	9.20R 6.13A	15.5	4.84
Fault Detector	6	3.94E5	9.91	15.2R 10.2A	23.0	11.7
MCAN Detector Commutated	2	2.44E6	0.338	0.820R 0.547A	1.75	5.08
Detector Fixed	3	2.44E6	0.639	1.23R 0.824A	2.26	1.74
Lamp Driver	3	2.10E5	7.31	14.3R 9.6A	26.3	4.16
FET Switch	5	1.75E7	0.177	0.286R 0.191A	0.452	0.331
Diode Array	2	9.50E5	0.868	2.11	4.50	2.34
Mode Logic	5	6.50E5	4.75	7.69	12.2	4.42
Timing Logic	4	6.50E5	3.53	6.15	10.3	4.45
Logic Sequencer	4	6.50E5	3.53	6.15	10.3	5.12
Mode Control	7	6.50E5	7.28	10.8	15.7	4.15
Word Masking Logic	2	6.50E5	1.27	3.08	6.58	4.60
Interface Driver[1]	12	3.50E6	2.58	3.43	4.54	6.84

* Failures/million hours

Table 10: **COMPARISON OF EXPERIENCED AND PREDICTED FAILURE RATES (Cont'd.)**

Hybrid Microcircuit	No. Fail.	Part Hour	Lower Limit*	Point Estimate*	Upper Limit*	New Prediction*
Data Buffer	17	2.30E6	5.86	7.39	9.32	2.91
Interface Driver$_2$	3	5.80E5	2.65	5.17	9.51	5.42
Buffer	2	5.80E5	1.42	3.45	7.38	2.67
Timing Control	6	6.51E5	6.01	9.23	14.0	4.78
Memory Hybrid Switch	31	1.40E8	0.187	0.221	0.262	0.347

* Failures/million hours

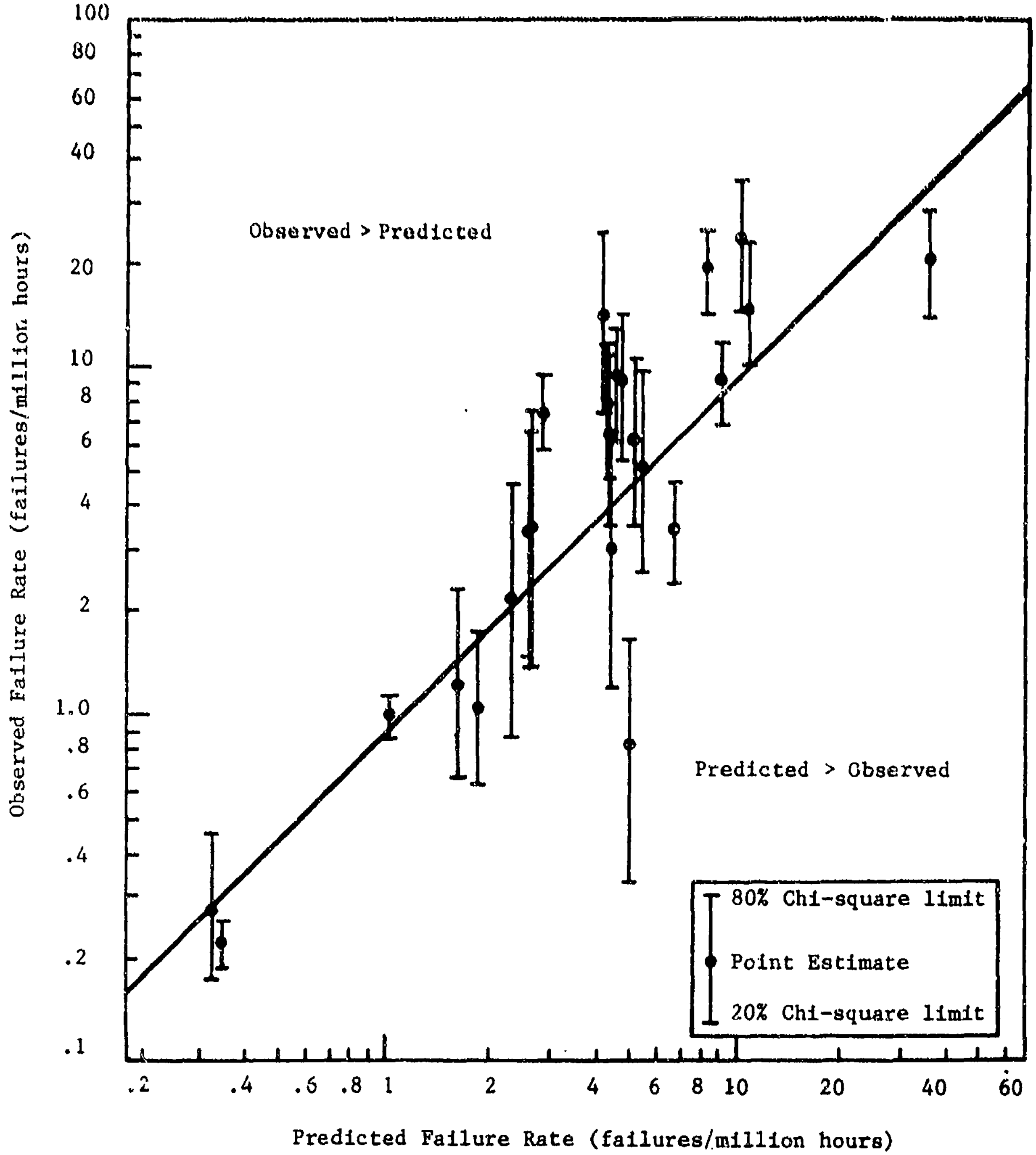


Figure 8: Proposed Predicted vs Observed Failure Rates

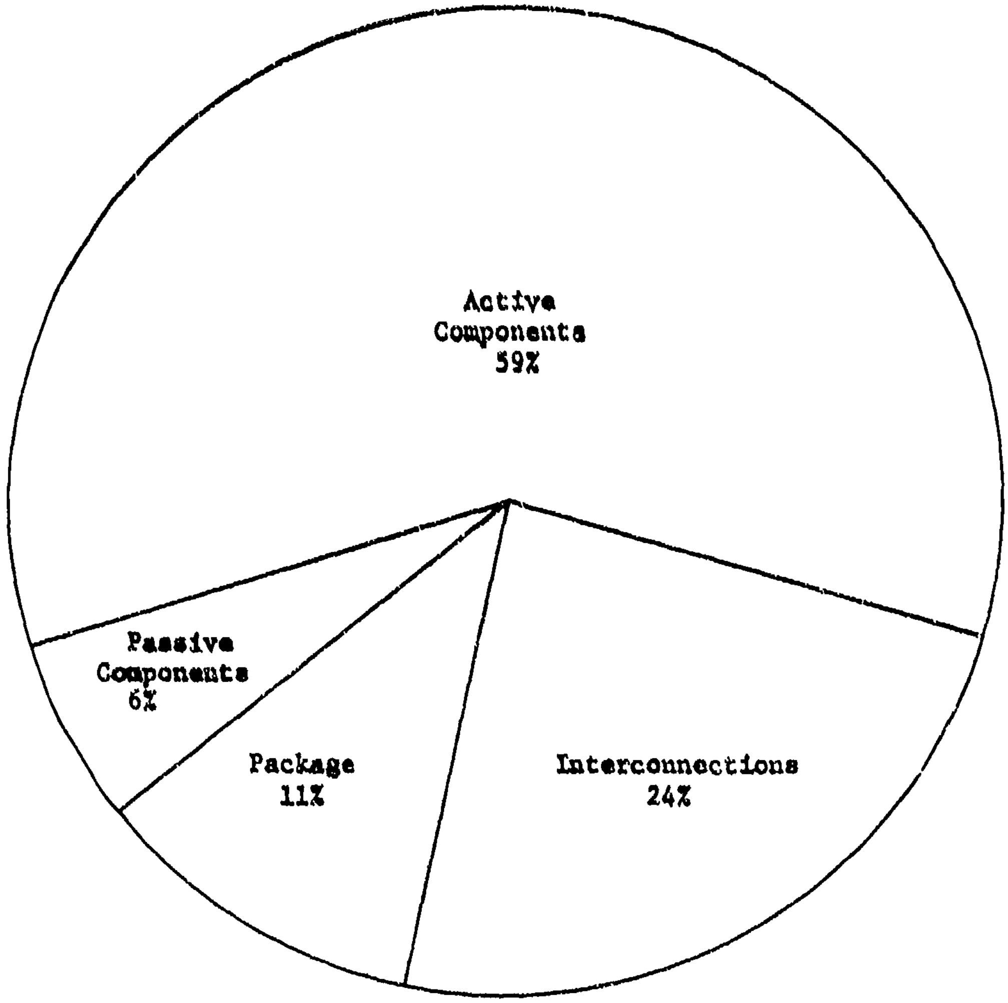


Figure 9: Base Failure Rate Contribution Distribution (New Hybrid Model)

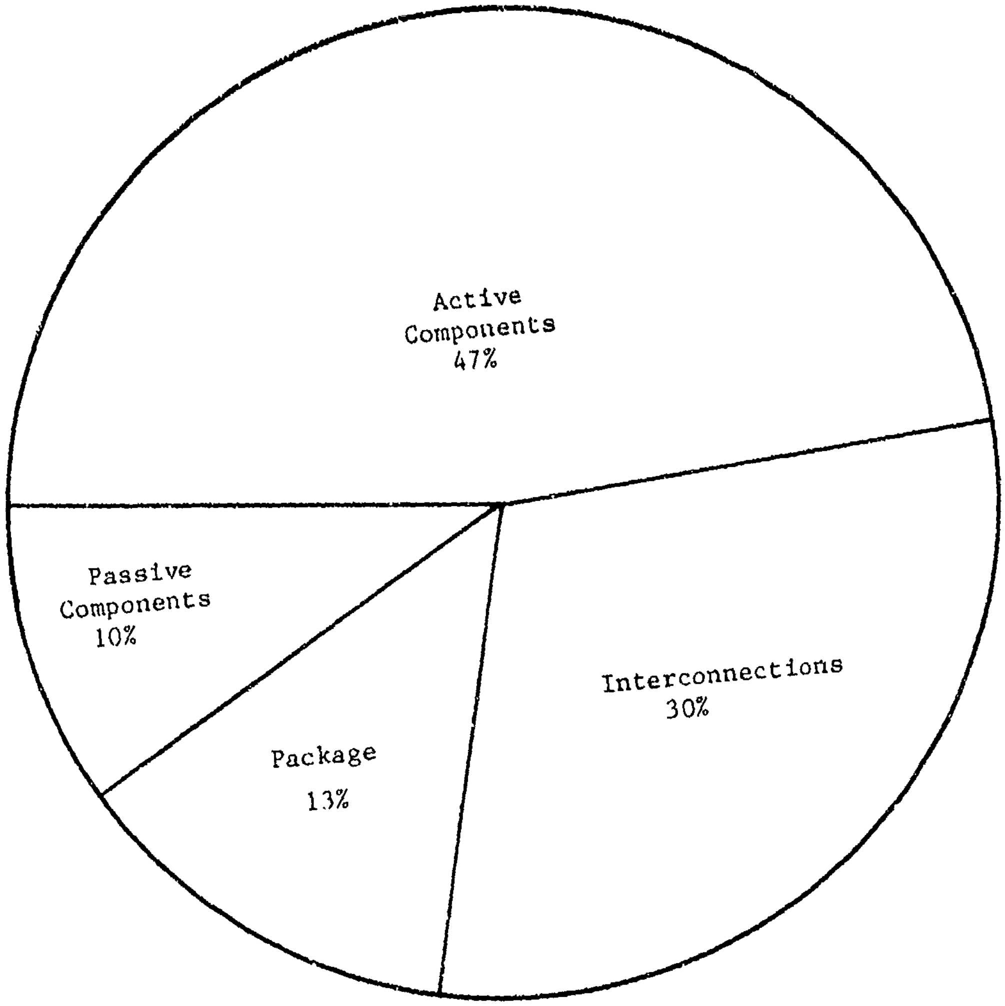


Figure 10: Reclassified Failure Distribution

Section VIII

CONCLUSIONS

Comparing the experienced failure rates of hybrid microcircuits to the values predicted by the method outlined in MIL-HDBK-217B, 20 September 1974, did not show a strong correlation between these values. Analysis of the model revealed that this was mainly due to several assumptions which had been made in an attempt to simplify the model. These assumptions were:

a. one environmental factor for all components

b. one temperature factor for all components

c. the contribution of interconnections to the failure rate will be adequately considered within the contribution of the components.

d. bipolar and MOS linear, bipolar beam lead, bipolar ECL and all other MOS integrated circuits will always fail twice as often as a comparable bipolar integrated circuit

It was found that the accuracy of the model could be greatly improved without substantially increasing the complexity of the model if these assumptions were not made.

The analysis of the available data indicated that the hybrid failure rate was not simply the sum of the failure contribution of the components. The density, interconnections per square inch, of the hybrid microcircuit was also found to be an important factor.

A new hybrid model was developed which generally predicted a failure rate which was very close to the failure rate experienced in the field. Comparing the prediction for a hybrid microcircuit to that predicted for an equivalent discrete circuit also showed results which were in keeping with the expected relative performance of these circuit construction techniques.

The hybrid microcircuit failure rate prediction model, as described herein, is very dependent on the models for discrete devices included in MIL-HDBK-217B. As any changes to these models will be reflected in the proposed hybrid model, the hybrid model will be somewhat flexible to the changes and new innovations in the microelectronic industry.

A good example of this is the current model in MIL-HDBK-217B for large scale integrated circuits. The current model predicts failure rates which are generally considered to be fairly pessimistic for devices with more than about 500 gates. A new LSI model is currently being developed and will, in effect, be included in the hybrid model as it is added to MIL-HDBK-217B.

Though one cannot hope for accuracy approaching the $\pm$ 0.1% of some of the calculations which were fit to the data in Table 10, this model should generally give a fairly good estimate of the failure rate which may be expected for a hybrid microcircuit operated under the specified conditions.

Appendix A

Data Solicitation Letter

DEPARTMENT OF THE AIR FORCE
HEADQUARTERS ROME AIR DEVELOPMENT CENTER (AFSC)
GRIFFISS AIR FORCE BASE, NEW YORK 13440

REPLY TO ATTN OF: RBRAC/4151

SUBJECT: MIL-HDBK-217B Hybrid Reliability Prediction Model Revision

TO:

1. As Preparing Activity for MIL-HDBK-217B, the Rome Air Development Center is responsible for monitoring and updating the various reliability prediction models. Recently a number of hybrid manufacturers and users have questioned the results obtained when exercising the hybrid model.

2. The following are areas of contention:

a. Predictions for particular functions when implemented in hybrid as compared to discrete technologies.

b. Difficulty in making calculations due to complexity.

c. Weighting given to constituent factors.

d. Factors not considered by the model.

3. RADC/RBRM has contracted with the Reliability Analysis Center (RAC) operated by the IIT Research Institute to provide assistance in making revisions to the model which can be substantiated by specific field experience and test data.

4. To assure the adequate consideration of all hybrid design approaches and application environments we are inviting industry to participate through data submittal. A sample of a typical data record and a blank summary form are attached to clarify the level of detail desired. However, the RAC is prepared to process data obtained in any format.

5. Any offering of data accumulated by your company or indication of potential data availability would be of great assistance in further developing the hybrid prediction model. Submittals should be addressed to Lee Mirth, Reliability Analysis Center, RADC/RBRAC, Griffiss AFB, NY 13441 (315-330-4151).

6. It is understood that this letter is not intended to be a commitment by the Government which could form the basis of a claim against the Government for compensation in connection with this matter.

D F Barber

D. F. BARBER
Chief, Reliability Branch
Reliability & Compatibility Division

2 Atch
1. Data Record Sample
2. Blank Summary Sheet

Appendix B

Worksheet for Hybrid Model

1. Hybrid substrate temperature _____ ^{o}C

2. Compute Active Component Failure Contributions

A. Integrated Circuits - Section 2.1

Number of Chips	$2\,[(C_1\,\Pi_{TI}) + (C_2\,\Pi_E)]\,\Pi_G$	$= \lambda_{PFC}$
		________
		________
		________
		________
		________
		________
		________
		________
	Total for ICs	= ________

Π_G = 0.6 if $\leq$400 gates, <4000 bits, or linear

= 0.8 if >400 gates or $\leq$4000 bits

B. Transistors - Section 2.2

Number of Chips	$\lambda_B\,\Pi_E\,\Pi_A\,0.2\,\Pi_R\,\Pi_{S2}\,\Pi_C\,0.4$	$= \lambda_{PT}$
		________
		________
		________
		________
		________
	Total for Transistors	________

C. Diodes - Section 2.2

Number of Chips	$\Pi_B \ \Pi_E (0.5) \Pi_R \ \Pi_A \ \Pi_{S2} \ \Pi_C$ (0.2)	$= \lambda_P$ ______
		______
		______
		______
		______
	Total for Diodes	______

3. Passive Components

A. Capacitors - Section 2.6

Number of Chips	Appropriate Model x 0.8	$= \lambda_P$ ______
		______
		______
		______
	Total for Capacitors	______

Environmental Factor (Π_E) = _____ (G_B, S_F, = 0.2; G_F = 1.0; A_I, N_S, G_M = 2.0; A_U; N_U = 3.0; M_L = 5.5)

Circuit Function Factor (Π_E) = _____ (1.0 digital, 1.25 linear or linear-digital combinations)

B. Number of Film resistors __X λ_R_____(Π_E)_____X(Π_F)_____ = _____

C. Number of bimetallic interconnections ___X(λ_I)___X(Π_E)___X(Π_F)___ = ___

Number of single metal interconnections ___X(λ_{I2})___X(Π_E)___X(Π_F)___ = ___

D. Inches of Package Seal ___, λ_S = ___X(Π_E)___X(Π_F)___ = ___

4. Base Failure Rate

Total for ICs_____ +

Total for Transistors ____ +

Total for Diodes ____ +

Total for Capacitors ____ +

Total for Bimetallic Interconnections ____ +

Total for Single Metal Interconnections ____ +

Total for Package Seal ____

= Base Failure Rate

5. Quality Factor (Π_Q) ___ (1.0 or 60 Table 3)

6. Number of Interconnections ____ ÷ (Substrate area ___ + .10) = Density __

Π_D = ____ (Table 4 corresponding to "Density" value)

7. Prediction (λ_p) = (λ_B) ____ X(Π_Q) ____ X(Π_D) ____

= ____ (failures/million hours)

Appendix C

List of Companies Contributing Data to this Study

1. AIL, Cutler-Hammer., Deer Park, NY
2. Circuit Technology Inc., Farmingdale, NY
3. Delco Electronics Division, Milwaukee, WI
4. Grumman Aerospace Corporation, Bethpage, NY
5. Hazeltine Corporation, Greenlawn, NY
6. Hughes Aircraft, El Segundo, CA
7. IBM Corporation, Owego, NY
8. Lear Siegler, Grand Rapids, MI
9. Lear Siegler, Maple Heights, OH
10. Litton Guidance & Control Systems, Woodland Hills, CA
11. Sperry Univac Computer Systems, St. Paul, MN

Appendix D

Comparison of 217B Model, Proposed Model and the Prediction for an Equivalent Discrete Circuit

Circuit Description	217B Model	Proposed Model	Discrete Model
Ladder Network 16 Thin Film Resistors (GF Environment)	0.068	0.038	0.026
Small Device 2 Si NPN and 2 PNP Transistors, 2 Si diodes 4 Film Resistors (AU Environment)	0.684	0.295	0.522
Small Device (Including IC) 1-2/4 buffer, 1-Si NPN Transistor 1 Film Resistor (AI Environment)	0.215	0.081	0.125
More Complex Device 28 Various Digital SSI ICs (AI Environment)	7.54	8.40	7.46
LSI Hybrid 16-2K NMOS RAM's	54.1	30.7	45.5
Linear Hybrid 3 Op Amps, 3 FETs, 4 Diodes 1 Capacitor (AU Environment)	9.15	3.20	3.98

Resistor Network - 16 thin film resistors (± 5%)
hybrid in soldered ceramic flat pack (0.85 x 0.268), A_S = 0.22, 32 interconnections (single metal)
discrete - MIL-R-39017 (R-level)
60% stress ratio, Ground Fixed, 40°C package temp. 1000 Ω, linear

Discrete

$$\lambda_{PR} = \lambda_b \, (\Pi_E \, \Pi_R \, \Pi_Q) \, N$$
$$= 0.0027 \, (5)(1)(0.1)16 = 0.0216$$
$$\lambda_{INT} + \lambda_{PWB} = N \, \lambda_s + \lambda_b \, N \, \Pi_E$$
$$= 32(0.00012) + 6E{-}6 \, (32)2 = 0.0042$$
$$\lambda_{Dis} = 0.0216 + 0.0042 = 0.0258$$

Old Hybrid

$$\Sigma N_{RT} \, \lambda_{RT} = 16(0.00025) = 0.004$$
$$\lambda_b = 0.02 + 0.22(0.0035) + 0.004 + 0.01(1.5) = 0.0398$$
$$\lambda_p = \lambda_p \, \Pi_E \, \Pi_Q \, \Pi_T \, \Pi_F$$
$$\lambda_p = 0.0398(1)(1)(1.7)1 = 0.068$$

New Hybrid

$$= 16(0.0001) + (0.000334)32 + 0.0055 = 0.018$$
$$\lambda_p = \lambda_P \, \Pi_E \, \Pi_F \, \Pi_D \, \Pi_Q$$
$$\lambda_p = 0.018(1.0)1.25(1.0)1.7 = 0.038$$

Small Digital Device - 2 SiNPN, 2 SiPNP, 2 SiGP diode, 4 thin film resistors, 50% stress ratio, Airborne Uninhabited, 40°C package, Class B, discrete active devices are JAN TXV, 1.8 watts max.
hybrid - A_s = 0.05, 15 pin solder sealed flat pack (1.8" seal), 17 interconnection (bimetal), digital

Discrete

$$\lambda_{Trans} = N\lambda_b \, \Pi_E \, \Pi_A \, \Pi_Q \, \Pi_R \, \Pi_{S2} \, \Pi_C$$
$$= 2(0.10) \, 40(0.7) \, 0.2(1.5) \, 0.64(1) = 0.108$$
$$= 2(.016) \, 40(0.7) \, 0.2(1.5) \, 0.64(1) = 0.172$$
$$\lambda_{Diode} = 2(0.0039) \, 40(0.7) \, 0.5(1.5) \, 0.70(1) = 0.115$$
$$\lambda_{Res} = 4(0.0024) \, 15(1) \, 0.1 = 0.014$$

No. Solder joints = 2(3) + 2(3) + 2(2) + 4(2) = 24

$$\lambda_{PWB} = 6E{-}6 \, (24) \, (20) = 0.0029$$

λ_I = 24(0.00012) = 0.00288

λ_p = 0.108 + 0.172 + 0.115 + 0.014 + 0.0029 + 0.00288 = 0.415

Old Hybrid

$\Sigma N_{DC}\ \lambda_{DC} + \Sigma N_{RT}\ \lambda_{RT}$ = 2(0.0053) + 2(0.0077) + 2(0.0048) + 4(0.00025) = 0.037

$\frac{N_E}{A_S} = \frac{34}{0.05}$

$\lambda_p = \lambda_b\ \Pi_E\ \Pi_Q\ \Pi_T\ \Pi_F$

λ_p = [0.02 + 0.037 + 0.05 (0.036) + 0.025] 6(1) 1.7(0.8) = 0.684

New Hybrid λ_b = 0.108(0.4) + 0.172(0.4) + 0.115(0.2) + [4(0.0001) + 17(0.000394) + 0.0026] 3.0(1.0) = 0.164

$\lambda_p = \lambda_b\ \Pi_D\ \Pi_Q$

λ_p = 0.164(1.0) 1.80 = 0.295

Small Digital Device (including IC)

1-bipolar 2/4 buffer, 1-SiNPN trans., 1 thick film resistor ± 5% (<100KΩ) 40% stress ratio, discrete resistor -R level MIL-R-39017, discrete IC-B-1, 40 C Junction, discrete trans. is Jan TXV Hybrid - 30 C package, 19 bimetallic interconnections, A_s = 0.063, solder seal can (1.3 in. seal) digital, air inhabited, thick film resistor

Discrete

λ_{IC} = 1(5) [0.0021(0.22) + 0.005(4)] 1.0 + 0.102

λ_{Trans} = 0.0079(25) 0.7(0.2)(1.5) 0.48(1) = 0.020

λ_{Res} = 0.0020(6.5)(1) 0.1 = 0.0013

λ_{PWB} = 6E-6(17)6 = 0.00061 no. solder connections = 12 + 3 + 2 = 17

λ_I = 17(0.00012) = 0.0020

λ_p = 0.002 + 0.00061 + 0.0013 + 0.020 + 0.102 = 0.126

Old Hybrid

$\lambda_b = \lambda_S + \Sigma\lambda_{DC}\ N_{DC} + A_S\ \lambda_C + \Sigma N_{RT}\ \lambda_{RT} + \lambda_{PF}\ \Pi_{PF}$

λ_b = 0.02 + 1(2) [0.0021(0.17) + 0.005(1)] 1 + (0.0053) + 0.069(0.063)+ 0.0005 + 0.015 = 0.056

λ_p = 0.056(4) 1(1.2) 0.8 = 0.215

New Hybrid

$\lambda_b \quad = \Sigma N_C \lambda_C \Pi_G + [N_R \lambda_R + \Sigma N_I \lambda_I + \lambda_S] \Pi_E \Pi_F$

$\lambda_b \quad = 0.6(2) \; [0.0021(0.22) + 0.005(4)] \; 1 + 0.4(0.0079) \; 25(0.7)$
$0.2(1.5) \; 0.48 + [0.0001 + 19(0.00023) + 0.0015] \; 2.0(1.0)$
$= 0.0445$

$\lambda_p \quad = \lambda_b \Pi_Q \Pi_D$, **Density = 10/0.063 + 0.10) = 117**

$\lambda_p \quad = 0.044(1)1.82(1) = 0.081$

More Complex Device

1 - 4 bit SR (50 gate), 2 - Dual JK FF (28 gate), 1-3/3 gate, 3-2/4 expander, 2- 16 bit decoder (56 gate), 3-FF (17 gates), 11 - hex inverters, 2 - 4 bit counter (72 gate), 3- 1/8 gate, 1- 2/4 buffer, air inhabited
Discrete - Class B-1, multilayer board, 70 C junction
Hybrid - Class B, 74 pin solder seal flat pack (6.2 in. seal), 60°C package A_s = 1.31, 410 interconnections (820 internal lead terminations), thin film

Discrete

(1) 1(5) [0.018(0.82) + 0.016(4)] (1) = 0.394

(2) 1(5) [0.012(0.82) + 0.013(4)] 1 = 0.618

1 (1) 5 [0.0027(0.82) + 0.0058(4)] 1 = 0.127

3 (1) 5 [0.0021(0.82) + 0.005(4)] 1 = 0.326

2 (1) 5 [0.020(0.82) + 0.017(4)] 1 = 0.844

3 (1) 5 [0.0088(0.82) + 0.011(4)] 1 = 0.768

11 (1) 5 [0.0043(0.82) + 0.0074(4)] 1 = 1.82

2 (1) 5 [0.023(0.82) + 0.018(4)] 1 = 0.909

3 (1) 5 [0.0013(0.82) + 0.0039(4)] 1 = 0.250

1 (1) 5 [0.0021(0.82) + 0.005(4)] 1 = 0.109

$\lambda_{PWB} = .0005 \; (414) \; 6 = 1.242$

$\lambda_I = 414(0.00012) = 0.0497$

$\lambda_p = 7.46$

Old Hybrid

$\Sigma \lambda_{DC} N_{DC} =$

1 (1) 2 [0.018(0.17) + 0.016]= 0.038

+2 (1) 2 [0.012(0.17) + 0.013] = 0.060

$+1\ (1)\ 2\ [0.0027(0.17) + 0.0058] = 0.013$

$+3\ (1)\ 2\ [0.0021(0.17) + 0.005] = 0.032$

$+2\ (1)\ 2\ [0.020(0.17) + 0.017] = 0.082$

$+3\ (1)\ 2\ [0.0088(0.17) + 0.011] = 0.075$

$+11\ (1)\ 2\ [0.0043(0.17) + 0.0074] = 0.179$

$+2\ (1)\ 2\ [0.023(0.17) + 0.018 = 0.088$

$+3\ (1)\ 2\ [0.0013(0.17) + 0.0039] = 0.025$

$+1\ (1)\ 2\ [0.0021(0.17) + 0.005] = 0.011$

$$\lambda_b = \lambda_S + \Sigma\lambda_{DC} N_{DC} + \lambda_C A_S + \lambda_{PF} \Pi_{PF}$$

$$\lambda_b = 0.02 + 0.603 + 0.034(1.31) + 0.01(4.68) = 0.714$$

$$\lambda_p = 0.714(4)\ 1(3.3)\ 0.8 = 7.54$$

New Hybrid

$\pi_G\ N_C\ \lambda_C =$

$(0.6)1\ (1)\ 2\ [0.018(0.82) + 0.016(4)]1 = 0.095$

$+(0.6)2\ (1)\ 2\ [0.012(0.82) + 0.013(4)]\ 1 = 0.148$

$+(0.6)1\ (1)\ 2\ [0.0027(0.82) + 0.0058(4)]\ 1 = 0.030$

$+(0.6)3\ (1)\ 2\ [0.0021(0.82) + 0.005(4)]\ 1 = 0.078$

$+(0.6)2\ (1)\ 2\ [0.020(0.82) + 0.017(4)]\ 1 = 0.203$

$+(0.6)3\ (1)\ 2\ [0.0088(0.82) + 0.011(4)]\ 1 = 0.184$

$+(0.6)11\ (1)\ 2\ [0.0043(0.82) + 0.0074(4)]\ 1 = 0.437$

$+(0.6)2\ (1)\ 2\ [0.026(0.82) + 0.019(4)]\ 1 = 0.234$

$+(0.6)3\ (1)\ 2\ [0.0013(0.82) + 0.0039(4)]\ 1 = 0.060$

$+(0.6)1\ (1)\ 2\ [0.0021(0.82) + 0.005(4)]\ 1 = \underline{0.026}$

1.50

$$\lambda_p = (\Sigma N_C\ \lambda_C\ \Pi_G + [\Sigma N_I\ \lambda_I + \lambda_S]\ \Pi_F\ \Pi_E)\ \Pi_Q\ \Pi_D$$

$$\lambda_p = \{1.50 + [\ 410(0.00131) + 0.234]\ 2\}\ 1\ (2.76) = \mathbf{8.40}$$

LSI Hybrid

16 - 2048 bit MNOS RAMs Air Inhabited
Hybrid - 376 interconnections (single metal, A_S = 2.27, thin film
Package seal = 6.9 solder, 74 pin metal flat pack, 40°C package case
Class B (Method 5008)
Discrete - Class B-1, 53°C junction temp., multilayer board

Discrete

$$\lambda_m = 16(1)\ 5\ [0.20(1.0) + 0.076(4)]\ 1.1 = 44.35$$

$$\lambda_{PWB} = 0.005(376)\ 6 = 1.13$$

$$\lambda_I = 376(0.00012) = 0.045$$

$$\lambda_p = 45.5$$

Old Hybrid

$$\lambda_b = \lambda_S + \Sigma N_{DC}\ \lambda_{DC} + A_S\ \lambda_C + \Pi_{PF}\ \lambda_{PF}$$

$$\lambda_b = 0.02 + 16(2)\ 2\ [0.20(0.32) + 0.076(1)]\ 1.1 + 2.27(0.0087) + 0.01(4.67) = 9.94$$

$$\lambda_p = 9.94(4)\ 1(1.7)\ 0.8 = 54.1$$

New Hybrid

$$\lambda_b = \Sigma N_C\ \lambda_C\ \Pi_G + [\Sigma N_I\ \lambda_I + \lambda_S]\ \Pi_E\ \Pi_F$$

$$\lambda_b = (16)1\ (2)[0.2(1.0) + 0.076(4)]1.1(0.8) + [376(0.000394) + 0.108]\ 2 = 14.7$$

$$\lambda_p = 14.7\ (1)\ 2.09\ (1) = 30.7$$

Linear Hybrid

3 - 741 op amps, 3-N channel FET's, 4 SiGp diodes, 1 ceramic capacitor,
60% SR, 60°C package, air uninhabited
Discrete - 70°C junction temp., capacitor-level P (rated to 125°C),
JANTXV FET and diode
Hybrid - 30 pin solder sealed flat pack (4.2 in. seal) Class B 62 bimetal
interconnections, A_s = 0.563, thin film

Discrete

$$\lambda_p = 3(1)\ 5\ [0.0061(3.5) + 0.014(6)] + 3(0.052)\ 40(0.2)\ 1.5(1) + 4(0.0082)\ 1(0.7)(1)(1)\ 0.5(40) + 0.018(10)\ 0.3 + 0.000006(43)\ 20 + 43(0.00012) = 3.98$$

Old Hybrid

$$\lambda_b = \lambda_S + \Sigma N_{DC}\ \lambda_{DC} + A_S\ \lambda_C + \Pi_{PF}\ \lambda_{PF}$$

$$\lambda_b = 0.02 + 3(2)\ [0.0061(0.24) + 0.014(1)]\ 2 + 3(0.063) + 4(0.0081) + 0.0004(5) + 0.563(0.0042) + 0.01(3\ 02) = 0.462$$

$$\lambda_p = 0.462(6)(1)3.3\ (1) = 9.15$$

New Hybrid

$$\lambda_b = \Sigma N_C\ \lambda_C\ \Pi_G + [\Sigma N_I\ \lambda_I + \lambda_S]\ \Pi_E\ \Pi_F$$

$$\lambda_b = 3\ (0.6)\ 1\ (2)\ [0.0061(3.5) + 0.014(6)] + 3\ (0.058)\ 40(0.2)\ 1.5(1)\ 0.4 + 4(0.0095\ 1(0.7)\ 1(1)\ 0.5(0.40)0.2 + 0.018(10)\ 1.0(0.8) + [62(0.00104)\ 0.089\ ]\ 3(1.25) = 1.94$$

$$\lambda_p = \lambda_b\ \pi_Q\ \pi_D$$

$$\lambda_p = 1.94(1.0)1.65 = 3.20$$

Appendix E

EXAMPLE ONE*

Comparison of MIL-HDBK-217B Predictions for a Discrete Circuit and an Equivalent Hybrid Microcircuit in two **Environments**

Circuit Description:

Ten 50 Gate Bipolar integrated circuits, junction temperature 125°C, MIL-M-38510, Class B

Discrete Circuit Prediction - multilayer board - reflow soldered
Missile Launch Application

$$\lambda_p = \Pi_L \Pi_Q \left(C_1 \Pi_T + C_2 \Pi_E \right) \text{ Qty} + \lambda_B N \Pi_E + \lambda_S N$$

$$= 1 (2) [0.018 (5.7) + 0.016 (10)] 10 + 5\text{x}10^{-4} (150) 20 + 0.00012 (150)$$

$$= 6.77 \text{ failures/million hours}$$

Space Flight Application

$$\lambda_p = 1 (2) [0.018 (5.7) + 0.016 (0.2)] 10 + 5\text{x}10^{-4} (150) 1 + 0.00012 (150)$$

$$\lambda_p = 2.21 \text{ failures/million hours}$$

Hybrid Circuit

$$\lambda_p = \lambda_B \Pi_T \Pi_E \Pi_Q \Pi_F$$

$$\lambda_B = \lambda_S + A_S \lambda_C + \Sigma \lambda_{RT} N_{RT} + \lambda_{DC} N_{DC} + \lambda_{PF} \Pi_{PF}$$

where:

$\lambda_S = 0.02$

$A_S = 0.5$ inches

$\lambda_C = 0.03$

$\Sigma \lambda_{RT} N_{RT} = 0$

$$\Sigma \lambda_{DC} N_{DC} = \Pi_L \Pi_Q (C_1 \Pi_T + C_2 \Pi_E) N$$

$$= 1 (2) [0.018 (0.34) + 0.016 (1)] 10$$

$$= 0.442$$

---

* This example was noted in a letter to the Commander, Rome Air Development Center, from N. Seiden, Singer Kearfott Division, 5 January 1976.

EXAMPLE ONE (cont'd)

$\lambda_{PF}\ \Pi_{PF}$ = 0.02

λ_B = 0.02 + 0.015 + 0.442 + 0.02
= 0.497

Missile Launch Application

λ_p = 0.497 (11) (10) 1 (0.8)

= 43.7 failures/million hours

Space Flight Application

λ_p = 0.497 (11) 0.2 (1) 0.8

= 0.875 failures/million hours

Conclusions:

1. For Space Flight applications, hybrids are 2.5 times better than a circuit from discrete components.

2. For Missile Launch applications, hybrids are 6.5 times worse than a discrete equivalent.

EXAMPLE TWO

Comparison of Prediction for a Discrete Circuit and an equivalent Hybrid Microcircuit in Two Environments using the **Proposed Model.**

Circuit Description:

Ten 50-gate bipolar integrated circuits, junction temperature 125°C, external package temperature 90°C MIL-M-38510, Class B Hybrid Substrate Area = 0.5 inches, Digital, Package perimeter = 3.0 inches, 165 interconnections, Au Wire.

Discrete Circuit Predictions:

Missile Launch Application = 6.67 failures/million hours

Space Flight Applications = 2.21 failures/million hours
(see Example One for calculations)

Proposed Hybrid Circuit Model

$$\lambda_p = \lambda_B \Pi_Q \Pi_D$$

$$\lambda_B = \{\Sigma N_C \lambda_C \Pi_G + [(N_R \lambda_R + \Sigma N_I \lambda_I + \lambda_S)] \pi_F \Pi_E\}$$

Missile Launch:

$$\lambda_p = \{1 (2) [0.018 (1.8) + 0.016 (10)] 0.6 (10) + [0.124 + 165 (0.00367)] 1.0 (5.5)\} 1.0 (2.69)$$

$$= \mathbf{17.0 \text{ failures/million hours}}$$

Space Flight:

$$\lambda_p = \{1 (2) [0.018 (1.8) + 0.016 (0.2)] 0.6 (10) + [0.124 + 165 (0.00367)] 1.0 (0.2)\} 1.0 (2.69)$$

$$\lambda_p = \mathbf{1.54 \text{ failures/million hours}}$$

Conclusions:

1. In a Missile Launch Application the discrete circuit is 2.5 times better than the hybrid microcircuit.

2. In a Space Flight Application the discrete circuit is 1.4 times worse than the hybrid microcircuit.

EXAMPLE THREE

Circuit Description:

Two 8-channel multiplexer (17 gates), 2-J-K Flip Flops (14 gates), 15 NPN transistors (Beam Lead) (Si), 5 ceramic capacitors, 5 Film Resistors (RL)
Multilayer, Ground Fixed, Digital, 90^{0}C junction, 50% stress ratio
Mil-M-38510 Class B-1 ICs, JANTX transistors, level M capacitors, resistors

Hybrid Description:

Substrate 0.88 x 0.85 in., 142 bimetallic interconnections per package, **Au Wire, 70 C Package Temperature, seal perimeter = 4.0 inches**

Discrete Calculation:

Resistors: $\lambda_p = \lambda_B \left(\Pi_E \Pi_R \Pi_Q\right)$

$\lambda_p = 0.0041\ (5.0)\ 1.0\ (1.0) = 0.0205$

Capacitors: $\lambda_p = \lambda_B \left(\Pi_E \Pi_Q\right)$

Transistors: $\lambda_p = \lambda_B \left(\Pi_E \Pi_A \Pi_Q \Pi_R\ \Pi_{S2} \Pi_C\right)$

$\lambda_p = 0.025\ (5)\ (0.7)\ (0.4)\ 1.0\ (0.75)\ 1.0 = \mathbf{0.0263}$

8 Channel Multiplexer: $\lambda_p = \Pi_L \Pi_Q \left((C_1 \Pi_T + C_2 \Pi_E\right))$

$\lambda_p = 1.0\ (5.0)\ [0.0087\ (1.8) + 0.011\ (1.0)] = 0.133$

JK Flip Flop: $\lambda_p = \Pi_L \Pi_Q \left(C_1 \Pi_T + C_2 \Pi_E\right)$

$\lambda_p = 1.0\ (5.0)\ [\ 0.0077\ (1.8) + 0.010\ (1.0)\ ] = \mathbf{0.119}$

Multilayer Board: $\lambda_p = \lambda_B\ N\ \Pi_E$

$\lambda_p = 5 \times 10^{-4}\ (124)\mathbf{2} = 0.124$

Reflow Solder $\lambda_p = 0.00012\ (124) = 0.0149$

Discrete Circuit Prediction:

$\lambda_p = 5(0.0205) + 5(0.024) + 15(0.0263) + 2(0.133) + \mathbf{2(0.119)}$
$0.124 + 0.0149$

$\lambda_p = \mathbf{1.26}$

Hybrid Microcircuit Calculation:

Film Resistors: 0.00015

Ceramic Chip Capacitors: (0.011) 2.0 (1.0) 0.8 = 0.018

EXAMPLE THREE (cont'd)

Transistors: 0.017 (5) 0.7 (0.2) 1.0 (0.64) (1.0) 0.4 = 0.00305

8 Channel Multiplexer: 1 (2) [0.0087 (.83) + 0.011 (1.0)] 0.6 = 0.0219

JK Flip Flop: 1 (2) [0.0077 (0.83) + 0.010 (1.0)] 0.6 = 0.0197

Interconnections: 0.00162

Package: 0.1191

Density: 142/(0.748 + 0.10) = 167., Π_D = 2.14

Π_E = 1.0

Hybrid Prediction: $\lambda_P = \lambda_B \Pi_Q \Pi_D$

$$\begin{aligned}\lambda_P &= \{15\ (0.00305) + 5\ (0.018) + 2(0.0219) + 2(0.0197) + \\ &\quad [\ 5(0.00015 + 142\ (0.00162) + 0.1191]\ 1.0(1.0)\}\ 1.0\ (2.14) \\ &= 1.22\end{aligned}$$

References:

1. Himmel, R.P., Hughes Aircraft Company, Pratt, I.H., U.S. Army Electronics Command, "Hybrid Microcircuit Failure Modes," Proceedings of the 1976 International Electronics Symposium.

2. Somerville, D.T., Rockwell International, "The Role of Hybrid Construction Techniques on Sealed Moisture Levels," Reliability Physics 1977.

3. Traeger, R.K., Sandia Laboratories, "Organics Used on Microelectronics: A Role of Outgassing Material and Effects," Proceedings of Electronic Components Conference 1977, pp. 408.

4. Lasch, K.B., Lynch, K.S., Raytheon Company, "Reliability Assessment of Mounted Ceramic Chip Capacitors Under Thermal Cycling Stresses," Proceedings of Electronic Components Conference 1975.

5. Himmel, R.D., Scrapple, R.Y., Keistev, F., Hughes Aircraft Company, "Large Area Hybrids - An Advanced Microelectronic Packaging Concept," Proceedings of Electronic Components Conference 1976.

6. Platz, E.F., IBM Components Division, "Reliability of Hybrid Microelectronics," Hopewell Junction, NY 1973.

7. Himmel, R.P., Koudounaris, A., Keister, F.Z., Hughes Aircraft Co., "Evaluation of Techniques for Sealing Large Hybrid Packages," RADC-TR-76-17, B011209L.